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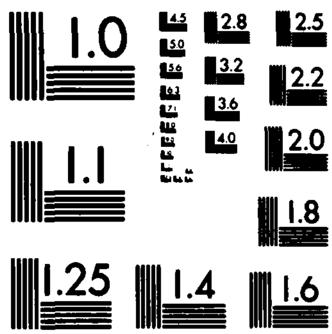

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RESEARCH AND DEVELOPMENT TECHNICAL REPORT
CECOM-82-C-J231

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500-WATT SOLID-STATE RF POWER AMPLIFIER AM-7209( )/VRC

M. Harris

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1502 72nd St. N.
St. Petersburg, Florida 33733

18 MARCH 1983

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The initial amplifier module specifications and system design concepts for the power amplifier are defined in this first quarterly report.

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1.0 INTRODUCTION

The development, fabrication, and test of three advanced development model 500-watt VHF power amplifiers to be used to increase the output of presently-deployed RT-524 (VRC-12) VHF radios and future equipment such as the SINCGARS-V equipment is documented in this report. The power amplifier, as defined in US Army Communications-Electronics Command contract DAAB07-82-C-J231, is a state-of-the-art stand-alone design utilizing a combination of the latest design techniques in RF elements, control circuits, packaging techniques, and amplifier architecture.

The initial amplifier module specifications and system design concepts for the power amplifier are defined in this first quarterly technical report, which is written in response to contract line item number 0004, data item sequence number C001 of the referenced contract. Also included in this report is a description of the completed contract effort to date and a listing of expected effort for the next reporting period.

2.0 AMPLIFIER SYSTEM ARCHITECTURE

The major initial effort in the design of the 500-watt power amplifier has concentrated on developing a unified approach to acheiving the desired power output while maximizing the efficiency of the amplifier and obtaining the highest practical reliability. To accomplish this objective, the amplifier has been partitioned into a number of significantly derated modules with a high degree of operating redundancy. Further, particular emphasis has been given to making certain that the amplifier operates at its specification limits under all conditions without requiring significant operating margins to insure that the requirements are met under environmental or operating extremes. This goal ia acheived through the use of a detailed control and feedback design with a microprocessor-based central controller to derate the amplifier operation as allowed. Operating together, the distributed amplifier approach with redundant, highly derated elements and the sophisticated control capability of the system result in a dependable, reliable amplifier.

Extending the capability of the amplifier, the information generated by the feedback control circuits to the processor used for power control purposes also contains significant BITE potential. This data, when combined with a logical internal test procedure, is capable of indicating external misapplication of the amplifier or internal failures and both changing operating characteristics to protect the unit while maintainng operation and signalling the condition to the operator. Efforts have been made to maximize the value of the control data generated within the amplifier for this purpose.

Finally, to maximize the application flexibility of the amplifier, each module circuit is designed for maximum performance from the available components and materials used. For example, the RF gain margins present in the power amplifier permit operation to lower-than-specified input power levels. This feature is incorporated in the design, permitting new, lower power equipment to drive the amplifier to full output, saving both primary power in the driver transmitter and reducing heat generated in the transmitter and dissipated in the power amplifier.

The remainder of Section 2 of this report describes the amplifier module partitioning, module interfaces, and module functions. Block diagrams and module electrical specifications define the capability and expected operation of the amplifier. At this time, the design of the power amplifier is being further refined and is settling toward its final specifications as the amplifier technology elements are being pursued. Therefore, although specifications and descriptions included in this report are tentative, the basic capabilities described and design goals listed represent the current design, and little change is anticipated in the design concept.

2.1 VHF POWER AMPLIFIER

The VHF power amplifier is a rugged, reliable, efficient, high performance unit capable of fully automatic push-to-talk operation with a variety of VHF driver transmitters. Operator interface with the amplifier is limited to connecting primary power and RF input and output cables, and turning the unit on. The operator controls are limited to an output power selection switch which permits selection of either the full 500-watt nominal output or a reduced 250-watt level and a display control switch. The amplifier display may be selected from the output forward power level, reflected power level, BITE code, or turned off. Frequency control and keying interfaces are internally controlled based on the RF drive signals applied.

The amplifier is composed of 17 major modules. Figure 2.1-1 is a block diagram showing the amplifier functional partitioning. Basically, the RF input is attenuated, then amplified by a variable gain driver amplifier and six paralleled output amplifiers before being filtered, sampled, and routed to the RF output connector. Support circuits include power supplies, RF power control loops, status measuring and reporting circuits, and the system processor. These circuits keep track of amplifier operation and control the RF output power level.

The following section lists the basic amplifier functional specifications, including inputs, outputs, and operator controls. This data represents data contained in the controlling equipment specification, CENCOMS 31-88 dated 2 March 1981, although more detailed information concerning certain characteristics such as output power versus operating conditions is provided.

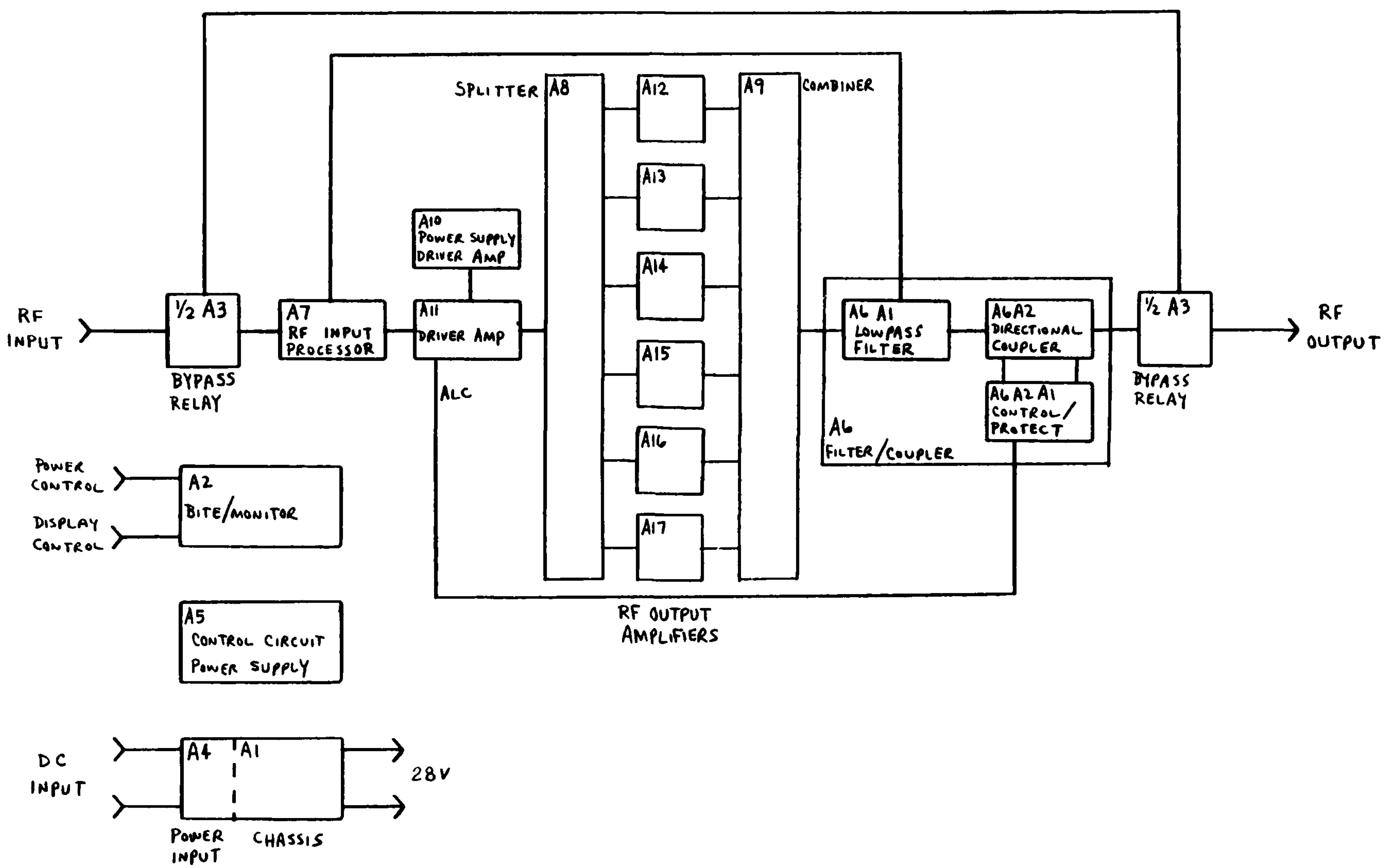


Figure 2.1-1. Power Amplifier Block Diagram

2.1.1 VHF POWER AMPLIFIER SPECIFICATIONS

The following specifications describe the 500-watt VHF power amplifier.

OPERATOR CONTROLS

POWER SWITCH
Turns on primary power to the unit. In off position, through connection between RF INPUT and RF OUTPUT connectors is established.

DISPLAY CONTROL SWITCH
1. Off   Blanks digital front-panel display.

2. Forward Power   Displays RF forward power output in watts.

3. Reflected Power   Displays RF reflected power output in watts.

4. BITE   Displays BITE error code. Initial indication is lighted decimal points in display.

POWER CONTROL SWITCH
1. 500 Watts   Selects 500-watt nominal forward output power.

2. 250 Watts   Selects 250-watt nominal forward output power.

OUTPUT DISPLAY
Three digit red LED hexadecimal display.
Power display - Indicates selected power level in watts with 3% accuracy at 50-watts or above.
BITE display - Three digit code indicating error source. Codes to be determined.

CIRCUIT BREAKER RESET
Press extended control shaft to reset.

RF INPUT

1. Frequency Range		30 - 88 MHz
2. Input Power		3 to 100 Watts
3. Input Impedance		50 ohms nominal
Input power over 15 watts		1.5:1 max VSWR
Input power under 15 watts		2.0:1 max VSWR
4. Duty Cycle		50 percent - 1 minute on, 1 off
5. Insertion Loss - Bypass Mode		
Power Off	Typical	0.2 dB
	Maximum	0.3 dB
Power On	Typical	0.4 dB
	Maximum	0.7 dB
6. Input Connector		Type "N"

RF OUTPUT

1. Power Level - Normal Conditions

	Min	Typ	Max	Units
500-watt Mode	500	512	535	Watts
250-watt Mode	225	250	280	Watts

2. Power Level - Stress Conditions

   Output power is reduced in response to operating conditions as listed below.

Load VSWR	See Figure 2.1-2	(dB)
	See Figure 2.1-3	(Watts)
Primary Input Voltage	See Figure 2.1-4	(dB)
	See Figure 2.1-5	(Watts)
Temperature	1 dB reduction at initial overheat indication. Power continues to reduce if temperature does not decrease.	

   All power reductions are additive. Load VSWR reduction is automatic for the loop control mode as shown in the Figure, and driven by the processor with a short delay to meet the processor control limits.

3. Electromagnetic Compatibility — MIL-STD-461A, Notice 4, Tailored. See Figures 2.1-6 and 2.1-7.

4. Output Connector — Type "N"

PRIMARY POWER INPUT

1. Voltage — 22 - 32 Volts, 27.5 Volts Nominal
Per MIL-STD-1275A (See Appendix A.3)

2. Current — 65 Amps Nominal, 80 Amps Maximum

3. Source Impedance — Resistive 0.1 ohms maximum
Inductive 100 uH maximum

4. Input Connector — MS90558N44N03P

5. Power Cable

Length	12 feet
Wire Size	2 AWG
Number of Conductors	2
Terminal Connector	FSN 5935-856-8426

6. Safety Ground — 1/4 - 28 stud provided for connection. Safety ground must be connected to apply power. Primary source is isolated from case except for 2 mA sense current.

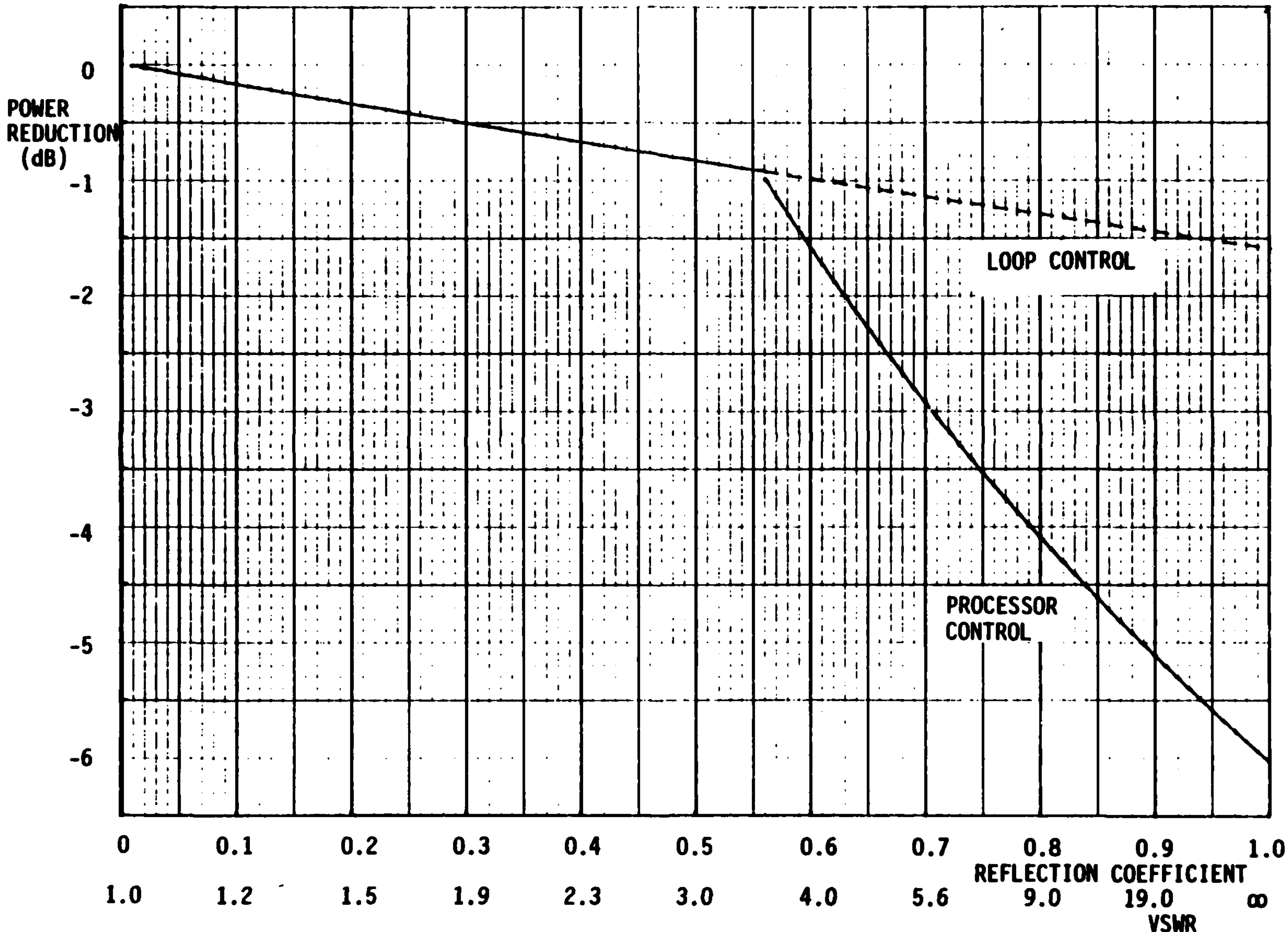


Figure 2.1-2. OUTPUT POWER REDUCTION VERSUS LOAD VSWR

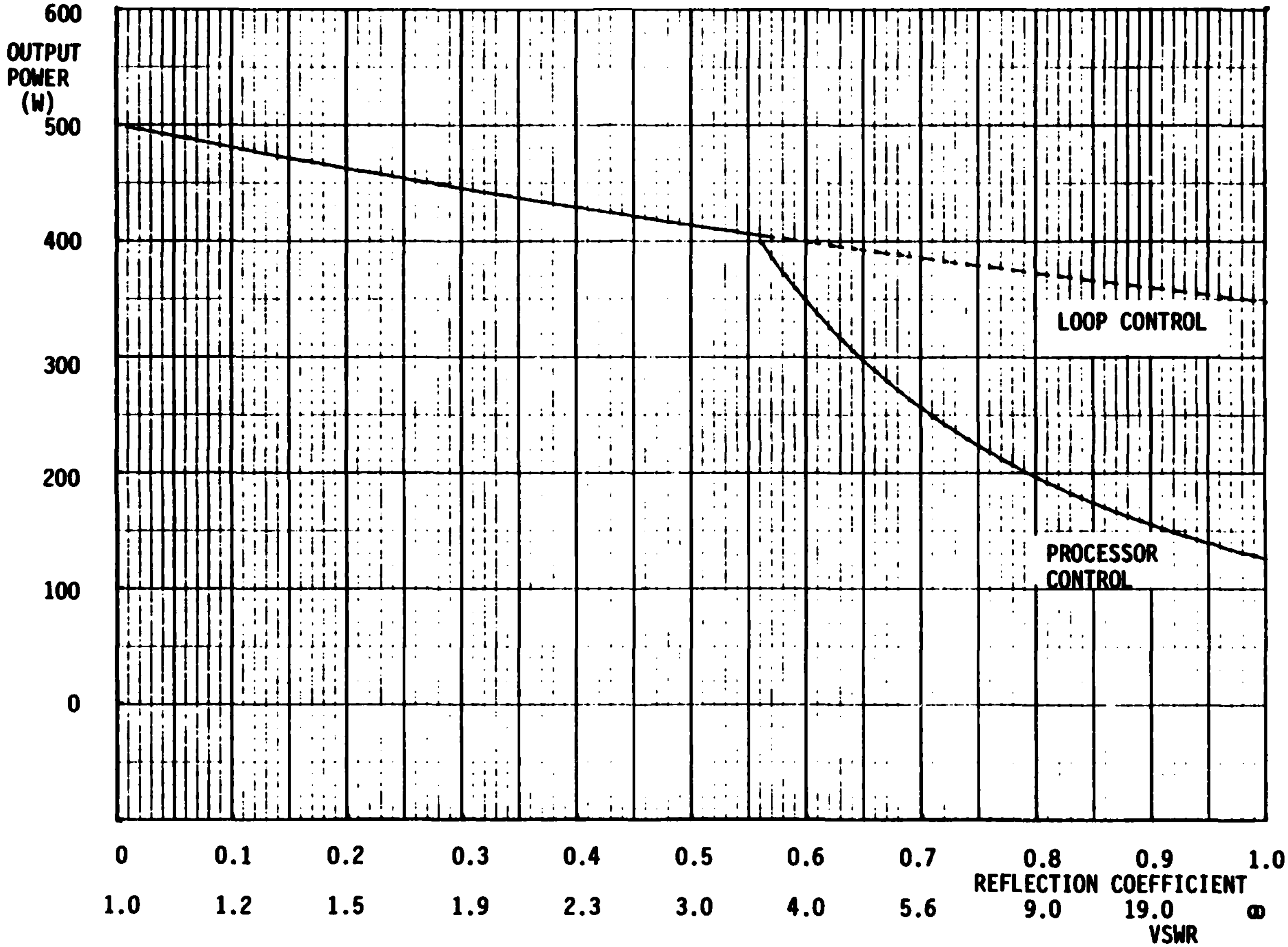


Figure 2.1-3. OUTPUT POWER CONTROL VERSUS LOAD VSWR

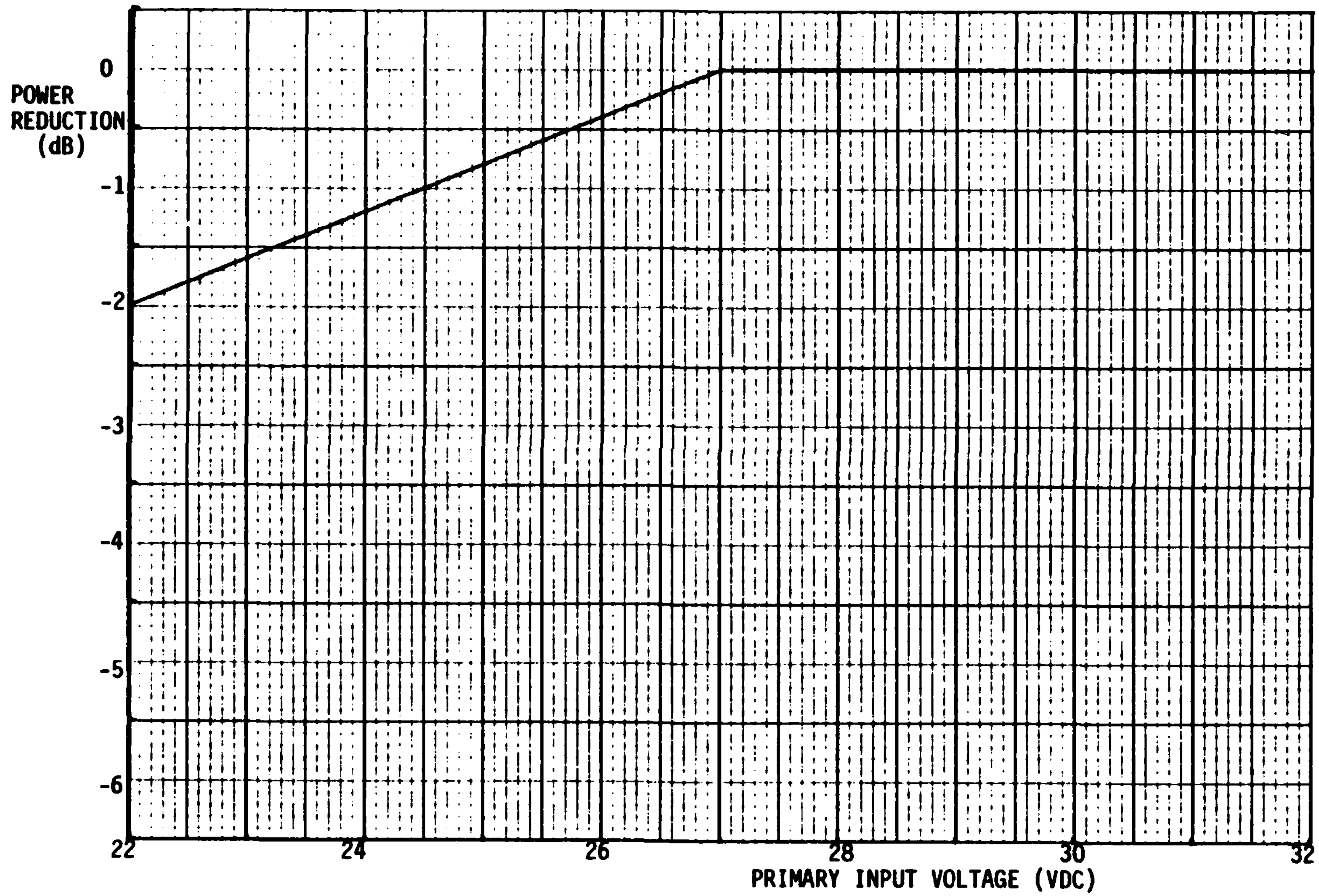


Figure 2.1-4. OUTPUT POWER REDUCTION VERSUS PRIMARY VOLTAGE

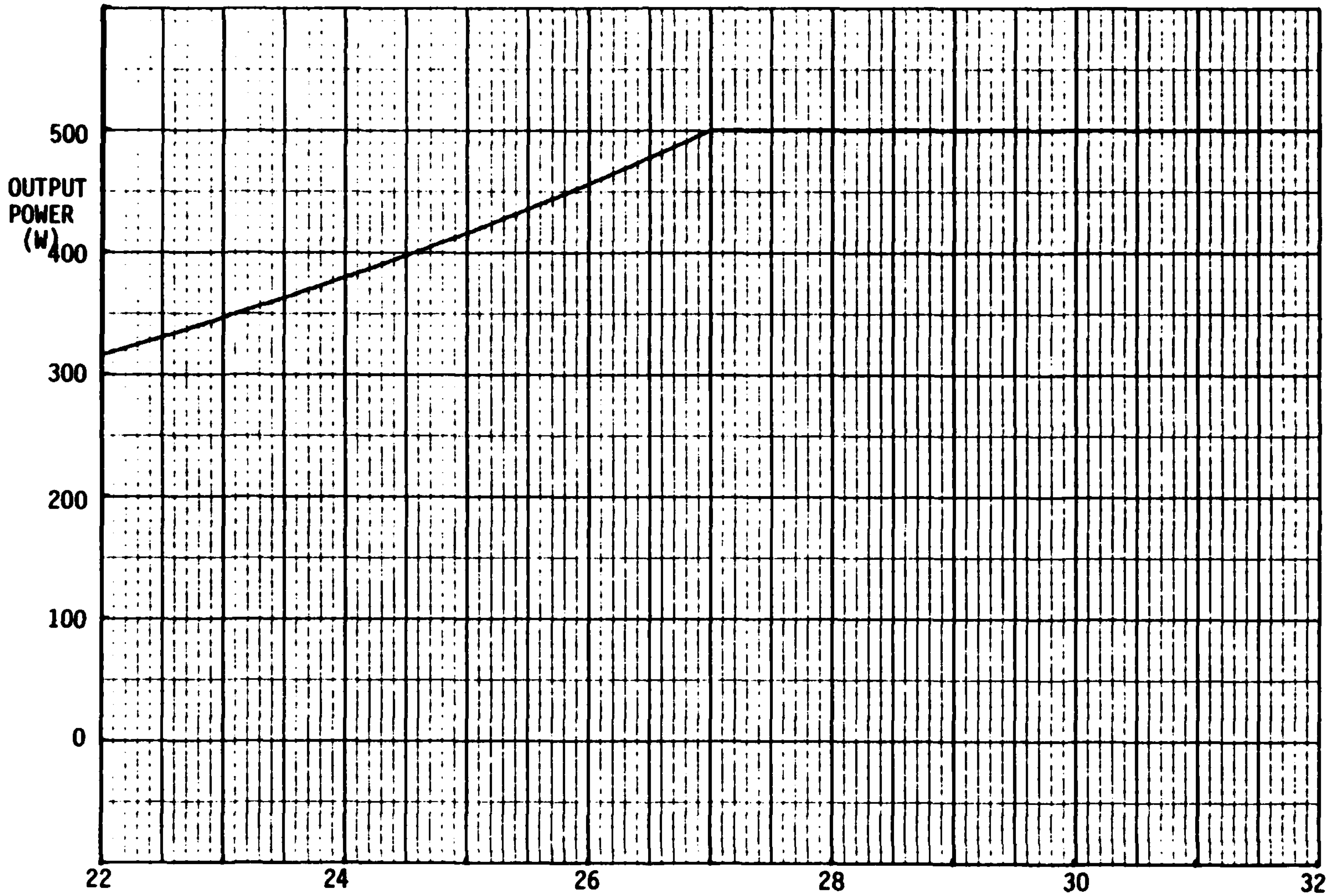


Figure 2.1-5. OUTPUT POWER CONTROL VERSUS PRIMARY VOLTAGE

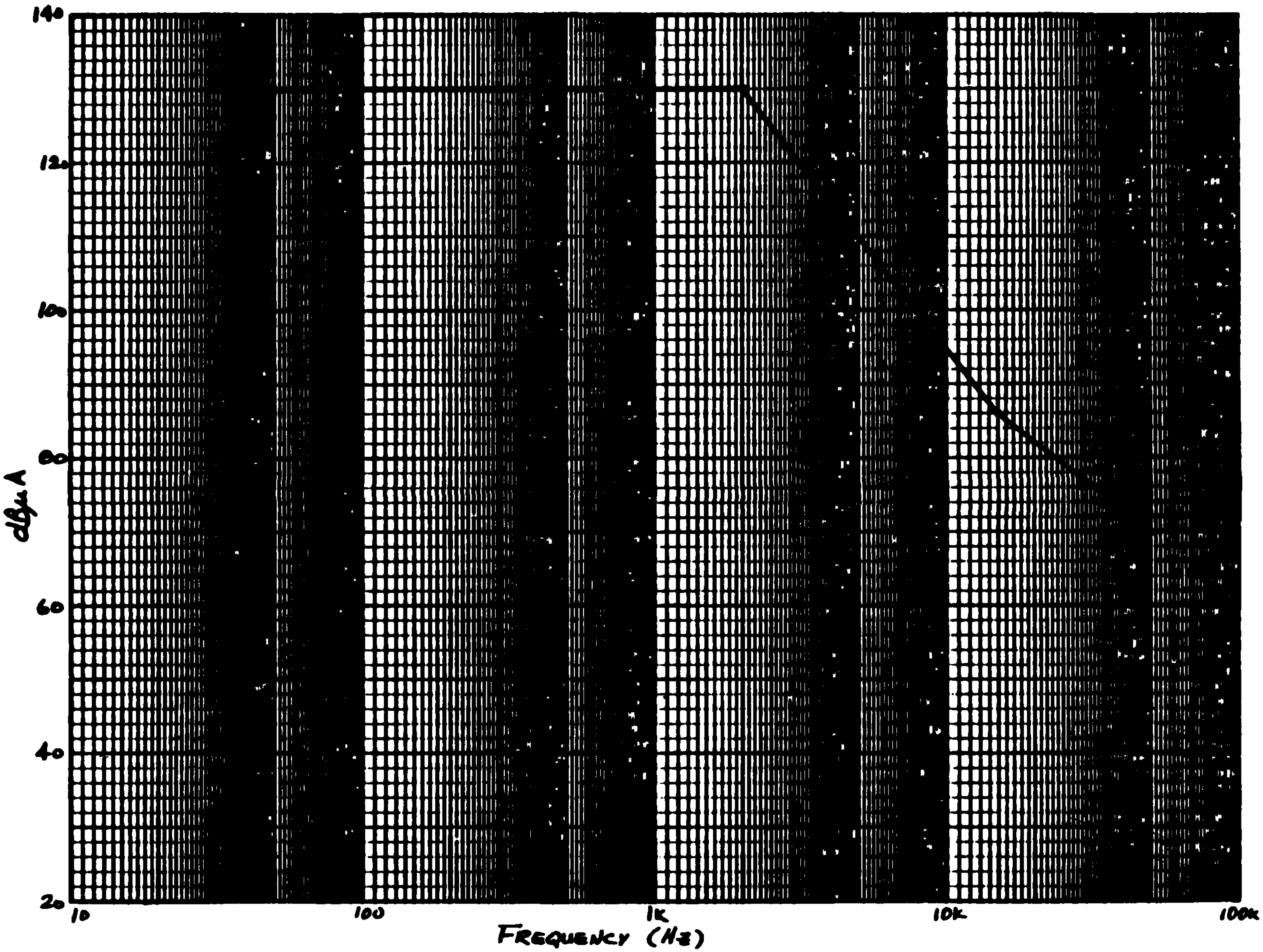


FIGURE 2.1-6 TAILORED CE01 NARROWBAND LIMIT

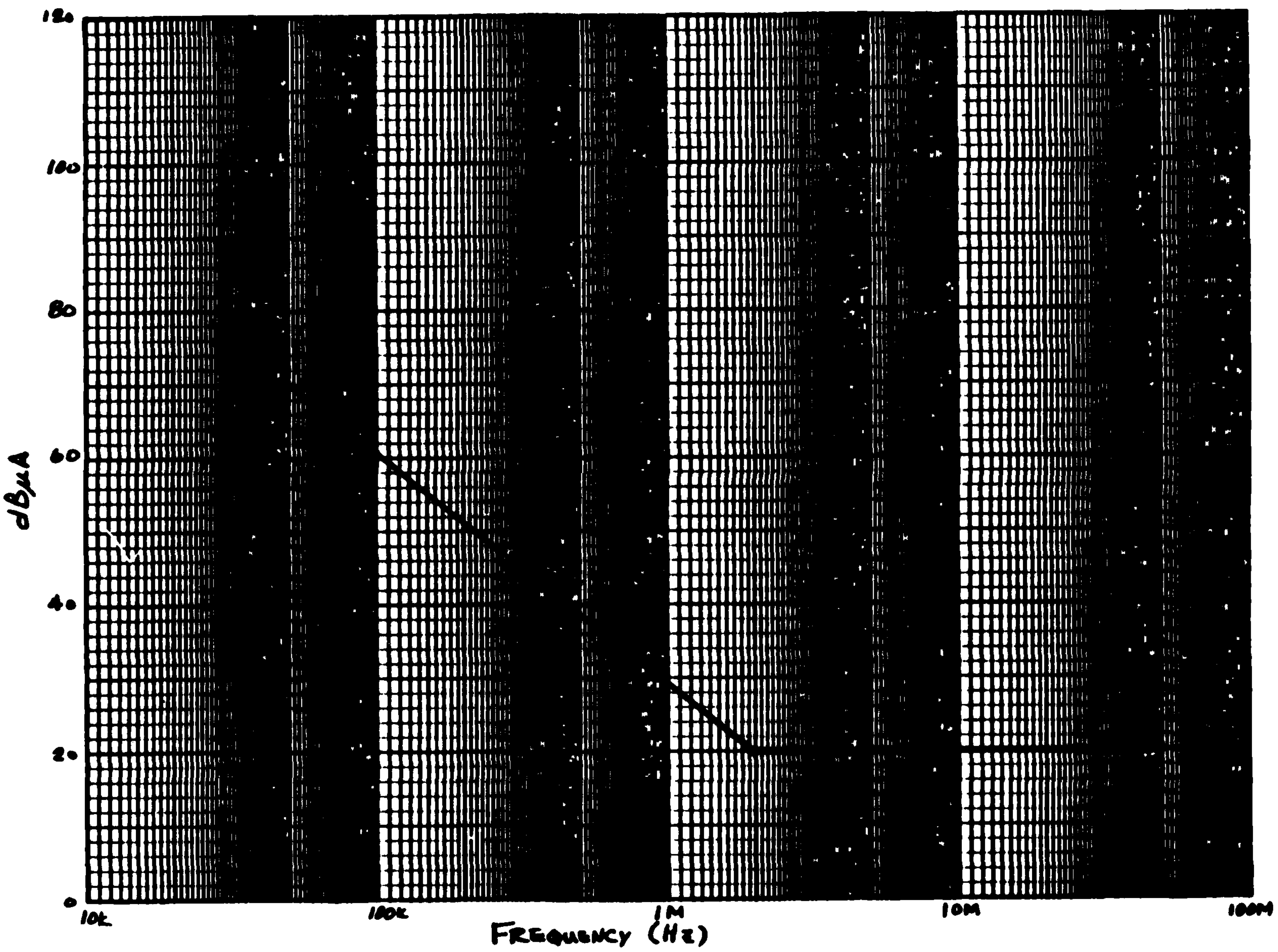


FIGURE 2.1-7 TAILORED CE04 NARROWBAND LIMIT

MECHANICAL SPECIFICATIONS

1. Temperature	-51 C to 52 C Operating -56 C to 71 C Storage
2. Humidity	MIL-STD-810 Method 507.1
3. Immersion	MIL-STD-810 Method 512.1
4. Vibration	MIL-STD-810 Method 514.2
5. Shock	MIL-STD-810 Method 516.2
6. Explosive Atmosphere	MIL-STD-810 Method 511.1
7. Size (Inches)	
Height	7.625
Width	21.625
Depth	13.375
8. Weight	75 pounds maximum
9. Cooling	Convection

2.2 POWER AMPLIFIER SUBASSEMBLY (CHASSIS) (A1)

In addition to providing a housing and heatsinking for the internal amplifier modules, the power amplifier chassis contains the electrical interconnect motherboard and RF cabling as well as the primary power input circuit and EMI filter.

The DC primary input voltage is first passed through a 150-amp circuit breaker to protect the vehicle power supply from amplifier failures. A low power, high voltage spike supressor next clips any high amplitude spikes from the vehicle supply. The input current is then switched by a power contactor, then again limited by a high power, low voltage surge supressor. Finally, an EMI filter provides filtering to internal power supply switching transients and signals to meet the requirements of MIL-STD-461B (See Appendix A.2).

The power contactor is controlled by the front panel switch and includes a circuit to insure that the chassis is connected to the input return line (as it normally is in vehicular installations). This circuit passes a small bias current through the safety ground to enable a pass transistor in the power contactor coil circuit. The input primary lines are otherwise totally isolated from the case in this and all other modules. This scheme provides both reverse polarity protection and operator safety under all combinations of possible fault conditions.

The input circuits are mounted within a closed cavity in the cast chassis front panel area. The EMI filter is mounted to the same casting wall to preserve EMI integrity.

The following section lists electrical parameters for the chassis circuitry. Figure 2.2-1 shows the power input circuit configuration.

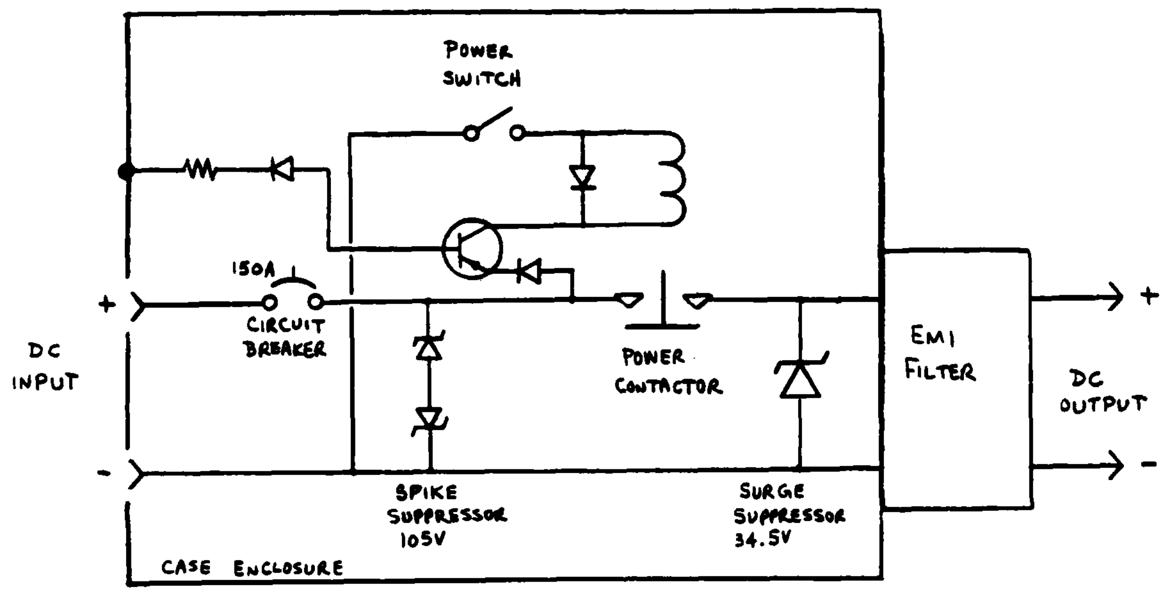


Figure 2.2-1 Input Power Circuits

2.2.1 CHASSIS ELECTRICAL REQUIREMENTS

The following specifications describe the power amplifier chassis electrical parameters.

POWER INPUT CIRCUITS

1.	Circuit Breaker	150 Amps
2.	Spike Supression (Bipolar)	105 Volts
3.	Surge Supression	34.5 Volts Nominal MIL-STD-1275A compatible (See Appendix A.3)
4.	Power Contactor	SPST 200-Amp Contacts
5.	Power Control	Front panel switch with reverse polarity protection to inhibit relay operation.
6.	Safety Ground Sense Curent	2 mA maximum
7.	EMI Filter	
	DC Power Dissipation	10 Watts maximum
	Filtering Limit	-120 dB at 200 kHz

RF CABLING

Interconnections to be made with minimum length cables.
At power levels below 150 watts, use RG-402 cable and SMA or equal connectors.
At power levels above 150 watts, use RG-401 cable and TNC connectors.

RF output amplifier modules (A12-A17) are connected with staggered-length cables with input cable lengths staggered in 6-inch minimum increments. The sum of input and output cable lengths are equivalent for all modules.

2.3 BITE/MONITOR (A2)

The BITE/monitor assembly is a microprocessor-based controller that performs all logic interface and module control functions to operate the power amplifier. In addition, the limited operator interfaces such as power level control, display selection, and display output are performed in this module.

The power amplifier system architecture has been set up such that the control and BITE information generated within the modules is transmitted via a common data communications bus. Individual modules in the amplifier are interrogated as required by first enabling the appropriate receiver or transmitter, then exchanging data over a common data bus. In essence, the amplifier modules become an extension of the microprocessor architecture. Therefore, the system controller contains address decoding circuits to enable the amplifier modules and a bus transceiver set for data exchange. The single data input not included in the bus system is the RF input detector signalling line. This input is used as a processor interrupt because of timing considerations when fast key response times are required, such as in frequency hopping systems.

To sample the major analog signals throughout the amplifier, a processor-driven analog-to-digital (A/D) converter is implemented. The significant data that needs critical processing is compared to fixed references in the corresponding module and signalled to the processor as a digital transition. However, data that is useful for BITE purposes or that can be updated at a relatively low rate is transferred on the analog conversion bus. This system uses a processor-mounted digital-to-analog converter and a low impedance analog reference is routed to all appropriate modules. On-card comparators signal the comparison to the analog output digitally to the processor to complete the conversion. This technique reduces the system complexity by eliminating a number of A/D converters and also improves noise immunity by eliminating a maze of small signals to be routed through the power amplifier.

Finally, the clock generator for the various system timing requirements is housed on the processor module. A 16 MHz master oscillator is the clock from which the processor clock, the phase-staggered power supply converters, and the input RF frequency counter signals are derived.

Figure 2.3-1 is a block diagram of the system BITE/monitor module. Major electrical requirements for this module are contained in the next section.

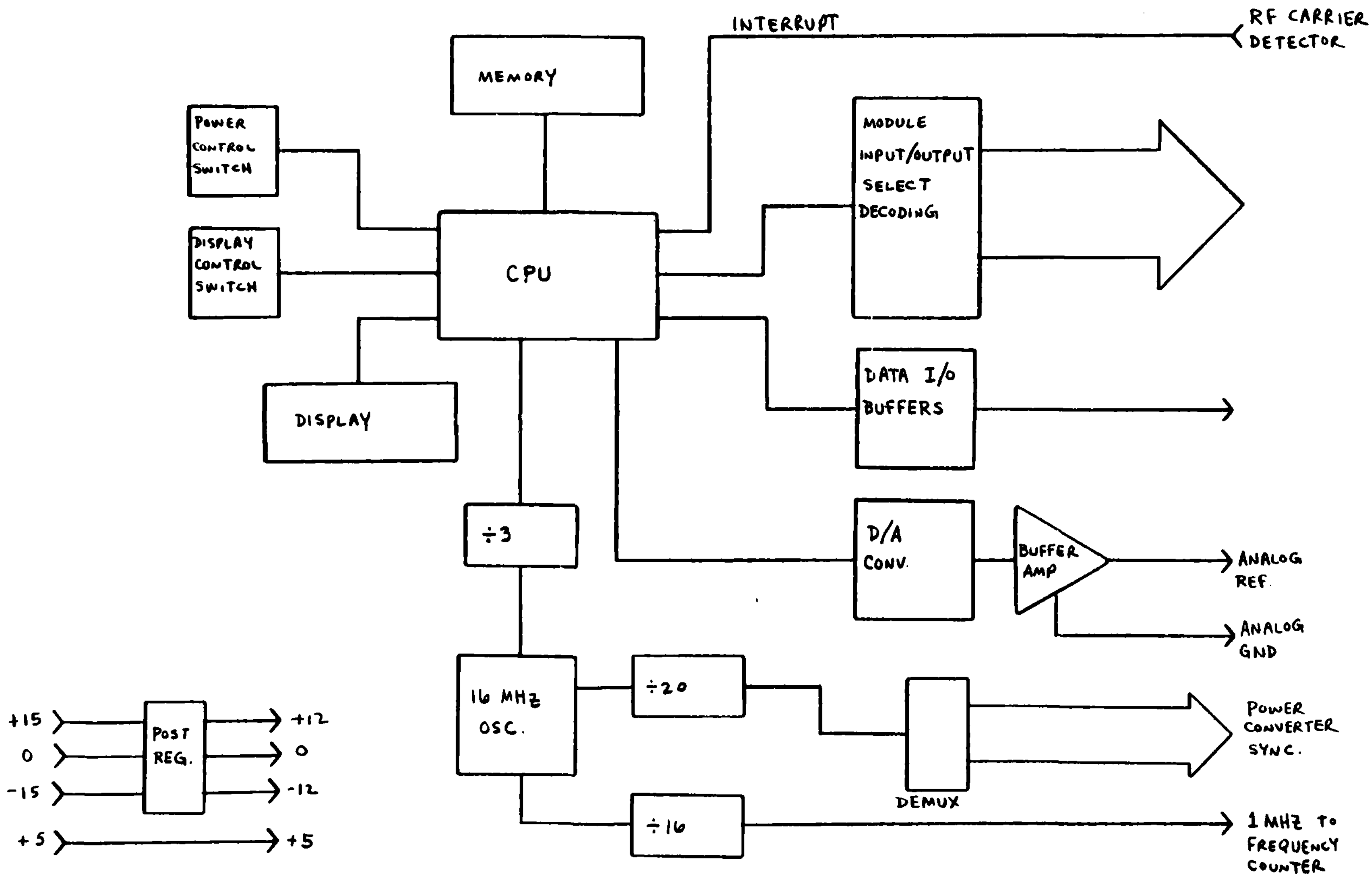


Figure 2.3-1 Bite/Monitor Circuit Block Diagram

2.3.1 SYSTEM CONTROLLER SPECIFICATIONS

Electrical specifications for the system BITE/monitor module are listed in this section.

OPERATOR INPUT/OUTPUT

DISPLAY CONTROL SWITCH

1. Off - Blanks digital front-panel display.
2. Forward Power - Displays RF forward power output in watts.
3. Reflected Power - Displays RF reflected power output in watts.
4. BITE - Displays BITE error code. Initial indication is lighted decimal points in display.

POWER CONTROL SWITCH

1. 500 Watts Selects 500-watt nominal forward output power.
2. 250 Watts Selects 250-watt nominal forward output power.

OUTPUT DISPLAY

Three digit red LED hexadecimal display.

Power display - Indicates selected power level in watts with 3% accuracy at 50-watts or above.

BITE display - Three digit code indicating error source. Codes to be determined.

	MINIMUM	TYPICAL	MAXIMUM	UNITS
CONTROL/DATA INPUTS/OUTPUTS				
1. Analog Reference (Input Voltage Measurement)				
Voltage	0		5	Volts
Load Impedance	4		7	kohms
			5000	pF
2. Source Select Decoding (Enables BITE/Control Sources)				
Level		TTL Compatible		
Load			6	LS TTL
Sense	Logic 1 = High Impedance Logic 0 = Signal Path Enabled			
3. Data Transmission Path - Transmit Mode				
Level		TTL Compatible		
Load			6	LS TTL
Sense	Defined By Selected Module			
4. Data Transmission Path - Receive Mode				
Level		TTL Compatible		
Load			6	LS TTL
Sense	Defined By Selected Module			
5. RF Input Detector Input - Signals Drive Presence				
Level		TTL Compatible		
Load			6	LS TTL
Sense	Logic 1 = No Signal Applied Logic 0 = RF Input Present			

	MINIMUM	TYPICAL	MAXIMUM	UNITS
FREQUENCY GENERATORS				
1. Master Oscillator				
Frequency		16.0		MHz
Temperature Drift/Accuracy		100		PPM
Duty Cycle			50	Percent
Level		TTL Compatible		
Load			5	LS TTL
2. Individual Converter Sync				
Frequency	180	200	220	kHz
Duty Cycle (Inverted Logic)	9	10	11	Percent
Level		TTL Compatible		
Load			2	LS TTL
3. Overall Converter Sync				
Phase Stagger		45		Degrees
4. Processor Clock				
Frequency	5.0	5.33	6.0	MHz
Duty Cycle			50	Percent
Level		TTL Compatible		
Load			5	LS TTL
5. Frequency Counter				
Frequency	0.999	1.000	1.001	MHz
Duty Cycle			50	Percent
Level		TTL Compatible		
Load			5	LS TTL

PROCESSOR BITE

Automatic self-test to be performed at power application and signalled by lighting all display segments. Display should be blanked during test.

	MINIMUM	TYPICAL	MAXIMUM	UNITS
DC POWER SUPPLY INPUTS				
1. Logic Supply				
Voltage	4.75	5.0	5.25	Volts
Current		2.5	3.0	Amps
2. 15-Volt Control Supply				
Voltage	14	15	16	Volts
Current		20	25	mAmps
3. -15-Volt Control Supply				
Voltage	-16	-15	-14	Volts
Current		20	25	mAmps

2.4 COAX RELAY/RF BYPASS (A3)

The coax relay/RF bypass module is an electromechanical RF relay bypass of the power amplifier to provide an interconnection between the driving transmitter and the output antenna when the power amplifier is unpowered or if a system failure prevents normal operation. The module includes an RF input coaxial relay, high power vacuum RF output relay, a bypass line RF detector, and a relay driver circuit.

The input relay is a sealed SPDT relay with coaxial terminations capable of switching up to 70 watts RF "hot" and 200 watts "cold". Because of the power level and equipment explosion requirements, a vacuum relay is used in the RF output line. A simple resistively-tapped diode detector is installed in the bypass line to signal the presence of an RF drive signal so that the relays can be commanded to switch only when drive is not applied. An integral drive circuit interfaces the relay coil drive current to a low level control signal.

The bypass module is assembled on a bracket and mounted to the front panel at the RF input and output connectors.

Electrical specifications for the bypass module are listed in the following section. Figure 2.4-1 is a block diagram of the module.

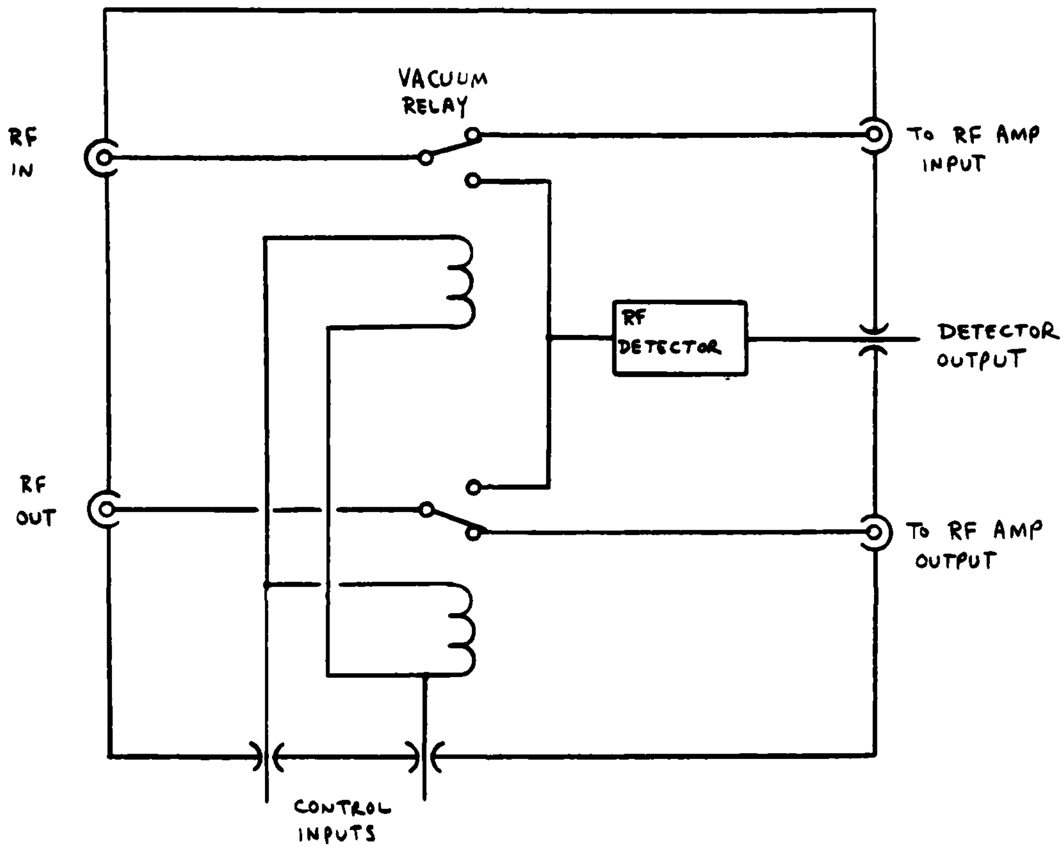


Figure 2.4-1 Fail-Safe Input Relay Circuit

2.4.1 COAX RELAY/RF BYPASS REQUIREMENTS

The following specifications apply to the coax relay/RF bypass module.

	MODE	MINIMUM	TYPICAL	MAXIMUM	UNITS
RF SPECIFICATIONS					
RF INPUT PORT					
Power Level	All	0	40	100	Watts
Insertion Loss					
To RF Amp Input	Enable		0.05	0.1	dB
To RF Output	Bypass		0.12	0.2	dB
Isolation					
To RF Amp Input	Bypass	40	50		dB
To RF Output	Enable	65	80		dB
RF OUTPUT PORT					
Power Level	All		550	600	Watts
Insertion Loss					
To RF Amp Output	Enable		0.07	0.1	dB
To RF Input	Bypass		0.12	0.2	dB
Isolation					
To RF Amp Output	Bypass	25	30		dB
To RF Input	Enable	65	80		dB
CONTROL SPECIFICATIONS					
DC SUPPLY INPUT					
Voltage		26	28	30	Volts
Current			100	120	mA
CONTROL INPUT					
Logic 0	Bypass				
Sink Current V=1 volt max.		8		10	mA
Logic 1	Enable				
Internal 3.3k ohm pull-up to 28 VDC					
DETECTOR OUTPUT					
RF Sense Level			1		Watt
Output Voltage			1	5	Volts

2.5 POWER INPUT ASSEMBLY (A4)

The power input assembly is a front-panel-mounted circuit that is the initial interface to the amplifier primary power source. The assembly contains only three major parts: the input power connector, the power control switch, and the input 150 amp circuit breaker. The components in this module connect to the power relay, transient protectors, and EMI filter of the chassis.

The power input assembly exists as a packaging convenience and has no particular specifications.

2.6 POWER SUPPLY - CONTROL CIRCUIT (A5)

The control circuit power supply generates all necessary voltages for operation of the various control, monitor, BITE, and primary power supply control circuits. The power supply is a switching regulator operated from the vehicular supply (See Appendix A.3) and is synchronized to a master clock to minimize conducted emissions. The supply configuration is similar to the other amplifier supplies (A10 and A12-A17) except that multiple secondaries are used to generate the needed voltages. In addition, a separate low power switching supply operates from the primary source with a totally isolated secondary to power the control circuit supply pulse width modulator and support circuits and maintain isolation between the high current primary source and the chassis.

The voltages from the supply are used for various purposes throughout the power amplifier. However, each voltage has a use that narrows the range and tolerance of the output and simplifies the design of the supply. For example, the highest current output of the supply is from the 5-volt source that is used to power the logic and control circuits in the amplifier. Because of the power levels present, this supply is tightly regulated and routed directly to the loads throughout the amplifier. A 150-volt and -5-volt supply is used to bias the PIN diodes in the various RF switches in the amplifier. Absolute voltage tolerance is not important for this use; however, ripple and noise must be kept low to avoid generating spurious signals transferred to the RF circuits and RF output. A dual +/- 15-volt supply is required for operational amplifiers, comparators, and similar analog circuits. To reduce noise and regulation requirements, and since the output power from this source is low, local regulation of this source to +/- 12 volts at the load is used in the amplifier modules. A 28-volt unregulated output from the supply is used to operate the mechanical bypass relays. Finally, a +12 to +15-volt supply powers the control circuits of the remaining power supply regulator modules.

Because the processor and control circuits operate from the control circuit power supply, this module is a critical element in the amplifier system and reliability is extremely important. Further, automatic BITE of this module is not possible because failures will result in shut-down of the BITE circuits. The use of this supply to operate the remaining RF module power supplies also insures that damage will be minimized in the event of a failure since all supplies will shut down in the event of a major failure of this module.

One control output generated in the control circuit power supply is the measurement of the primary power source DC level and ripple voltage. This information is signalled to the system controller through comparison to a external reference voltage and is used to reduce the RF output power when the input voltage falls below nominal limits.

The control circuit power supply is mounted within the amplifier case and is heatsinked to the case top cover to remove heat generated within the supply.

Figure 2.6-1 is a block diagram of the power supply and Table 2.6-1 contains a listing of the supply loads and locations. The following section lists electrical specifications for the module.

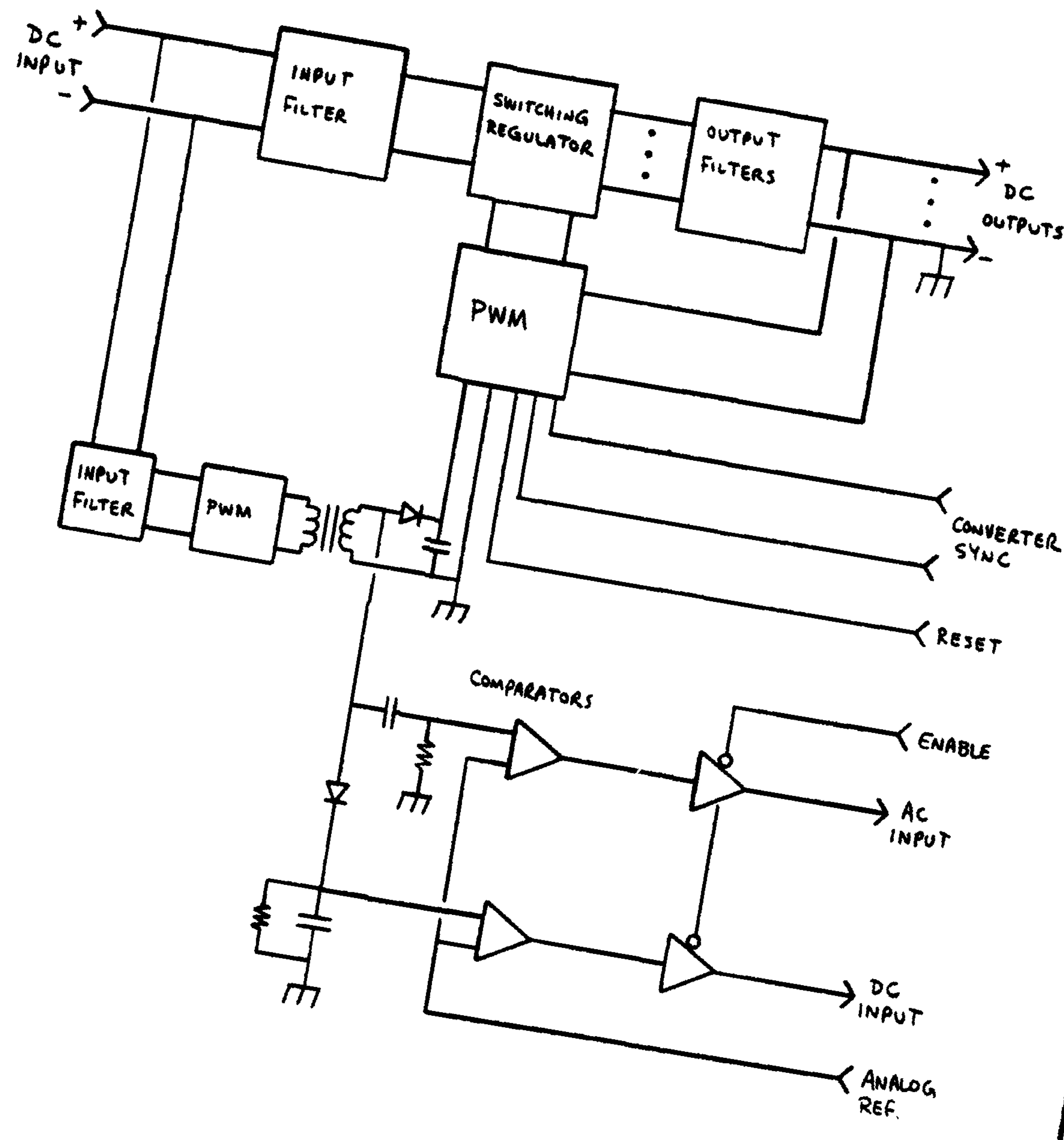


Figure 2.6-1 Control Circuit Power Supply

Table 2.6-1 Control Circuit Power Supply Load Currents

	Supply Voltage (V)						
MODULE	+5	-5	+150	+15	-15	+12	+28
A2	3000			25	25		
A3							120
A6	270	1500	1	75	75		
A7	270	1500	1	75	75		
A10						150	
A12-A17						150 x6	
TOTALS	3470	3000	2	150	150	1050	120
POWER (W)	17.35	15	0.3	2.25	2.25	12.6	3.4

TOTAL POWER (W) = 53.2

NOTE: All currents listed in milliamps.

2.6.1 CONTROL CIRCUIT POWER SUPPLY REQUIREMENTS

The following specifications describe the control circuit power supply.

CONFIGURATION	Switching, coupled-inductor, current-driven buck converter.
SWITCHING FREQUENCY	100 kHz

	MINIMUM	TYPICAL	MAXIMUM	UNITS
DC OUTPUTS				
1. Logic Supply				
DC Voltage	4.75	5.0	5.25	Volts
Ripple Voltage			0.1	Volts
DC Current			3.5	Amps
2. PIN Diode Forward Bias Source				
DC Voltage	-6	-5	-4	Volts
Ripple Voltage			20	mVolts
DC Current			3.0	Amps
3. PIN Diode Reverse Bias Source				
DC Voltage	130	150	170	Volts
Ripple Voltage		2	5	mVolts
DC Current			2	mAmps
4. Control Circuit Positive Source				
DC Voltage	14	15	16	Volts
Ripple Voltage			50	mVolts
DC Current			150	mAmps
5. Control Circuit Negative Source				
DC Voltage	-16	-15	-14	Volts
Ripple Voltage			50	mVolts
DC Current			150	mAmps
6. Power Supply Controller Source				
DC Voltage	8	12	15	Volts
Ripple Voltage			100	mVolts
DC Current			1.05	Amps
7. Bypass Relay Source				
DC Voltage	24	28	32	Volts
Ripple Voltage			200	mVolts
DC Current			120	mAmps

DC INPUTS

1. Primary Power Source[1]

Differential DC Voltage	21.5	27.0	32	Volts
Ripple Voltage (50 Hz-200 kHz)			14	Volts pk-pk
DC Input Current			3.9	Amps
Supply Efficiency	65	70		Percent

1 Input voltage per MIL-STD-1275A (See Appendix A.3).
Voltage at supply processed by input circuits and EMI filter (A4 and A1FL1).
Input DC circuit to be totally DC isolated from case ground.

CONTROL INPUTS

1. Clock (Converter Sync)

Frequency	180	200	220	kHz
Duty Cycle	9	10	11	Percent
Level		TTL Compatible		
Load			2	LS TTL

2. Analog Reference (Input Voltage Measurement)

Voltage	0		5	Volts
Load Impedance	20		33	kohms
			1000	pF

3. Output Select (Enables BITE Outputs)

Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = High Impedance			
	Logic 0 = BITE Outputs Enabled			

4. Supply Reset (Permits Recovery Attempt From Auto-Shutdown)

Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Normal			
	Logic 0 = Reset			

BITE OUTPUTS[1]

1. DC Input Voltage (Signal Comparison To Analog Reference)

Input Attenuation Factor		6		
Signal Threshold		0.0		Volts
Output Level			TTL Compatible	
Output Load			4	LS TTL
Sense	Logic 1 = Voltage Below Reference			
	Logic 0 = Voltage Exceeds Reference			

2. AC Input Voltage (Signal Comparison Peak Voltage To Analog Reference)

Input Attenuation Factor		4		
Signal Threshold		0.0		Volts
Output Level			TTL Compatible	
Output Load			4	LS TTL
Sense	Logic 1 = Voltage Below Reference			
	Logic 0 = Voltage Exceeds Reference			

1 Outputs are Tri-State TTL and are enabled by OUTPUT SELECT line.
All outputs are high impedance unless selected.

2.7 FILTER/DIRECTIONAL COUPLER (A6)

The low pass filter and directional coupler module contains the final RF output bandpass shaping and power control circuits for the power amplifier. The combined output of the six RF power amplifiers is first passed through the switched low pass filter set to remove harmonic signals generated during the amplification process. Because the frequency band is over one octave, two low pass filters are used, with the proper filter selected by the control processor based on the input frequency counter output. An RF directional coupler follows the filter assembly to sample the output forward and reflected power components. The sampled power signals are detected, and a high gain power control loop and power reference generator in this module create the feedback control signal to the variable attenuator in the driver amplifier to control the output power level.

The lowpass filter and switch assembly includes two purchased filters: one for operation with 30-52 MHz fundamental signals and the other for the 52-88 MHz band. The input switch routes the amplifier output through either filter, while the output switch selects either a filter output or the amplifier bypass path from the RF input processor. High power series-shunt PIN diode switches select the proper RF path, and interface circuits create the proper bias levels from TTL compatible command inputs. To speed the switching transition times, direct pull-up or pull-down circuits to the bias supplies sequenced by a control circuit to avoid simultaneous conduction are used. Figure 2.7-1 is a block diagram of this circuit and Section 2.7.1 contains the electrical specifications.

The output coupler is implemented as a stripline backward-wave coupled line assembly with capacitively-compensated outputs to obtain a leveled output response. The circuit is built on a low loss controlled dielectric substrate and sized to obtain the desired coupling factor and to handle the power levels required. Section 2.7.2 contains specifications for the coupler.

Finally, the control and protect circuits consist of a number of wide bandwidth amplifiers to generate error signals for power correction and various circuits for status feedback and BITE generation to the system controller. Section 2.7.3 contains the electrical specifications for this portion of the output module, and Figure 2.7-4 is a block diagram of the directional coupler and the control circuits.

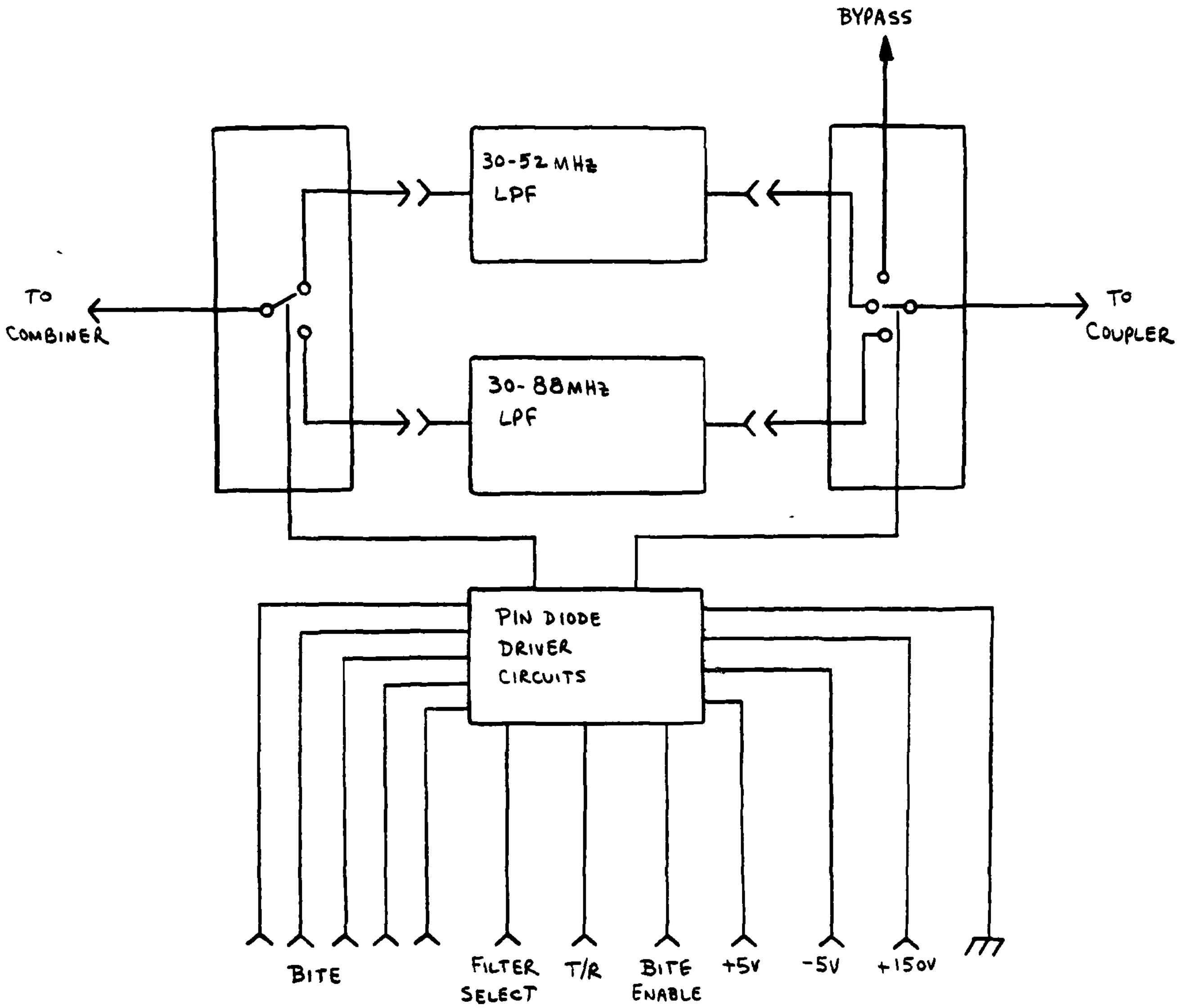


Figure 2.7-1 Harmonic Filter Subassembly

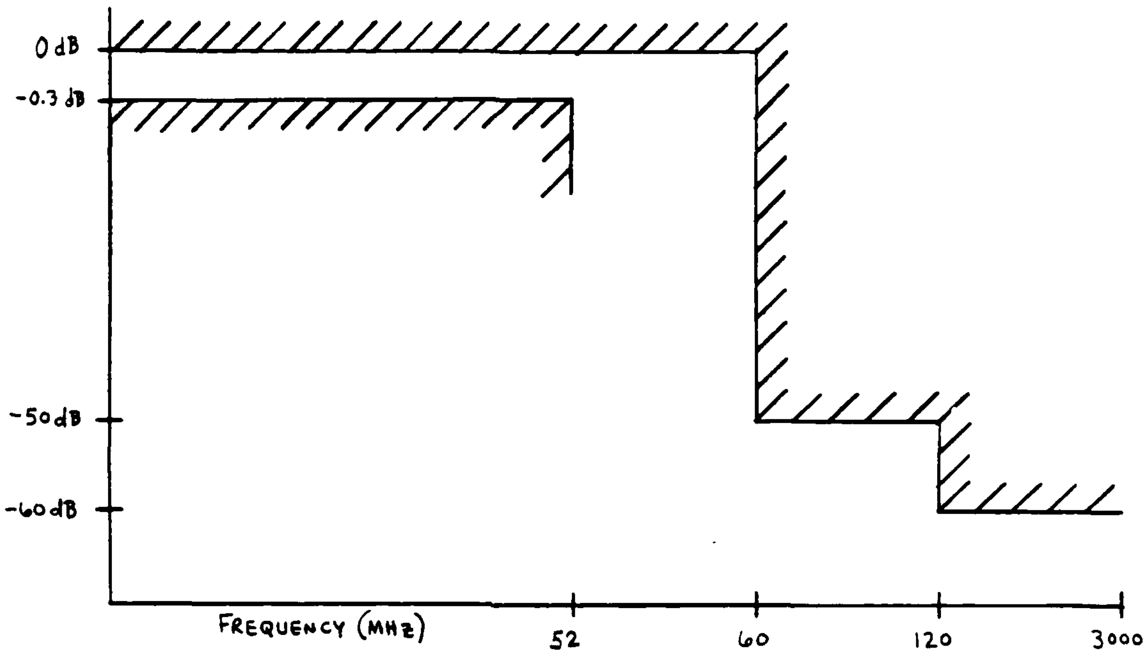


Figure 2.7-2 Low Band Filter Bandpass Characteristics

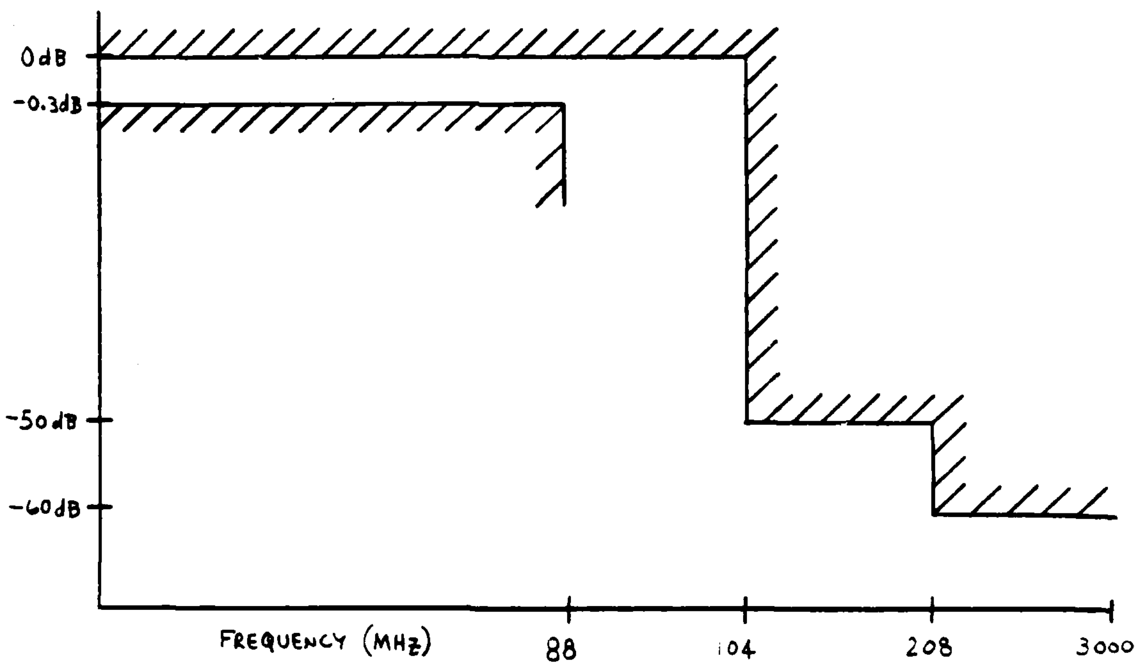


Figure 2.7-3 High Band Filter Bandpass Characteristics

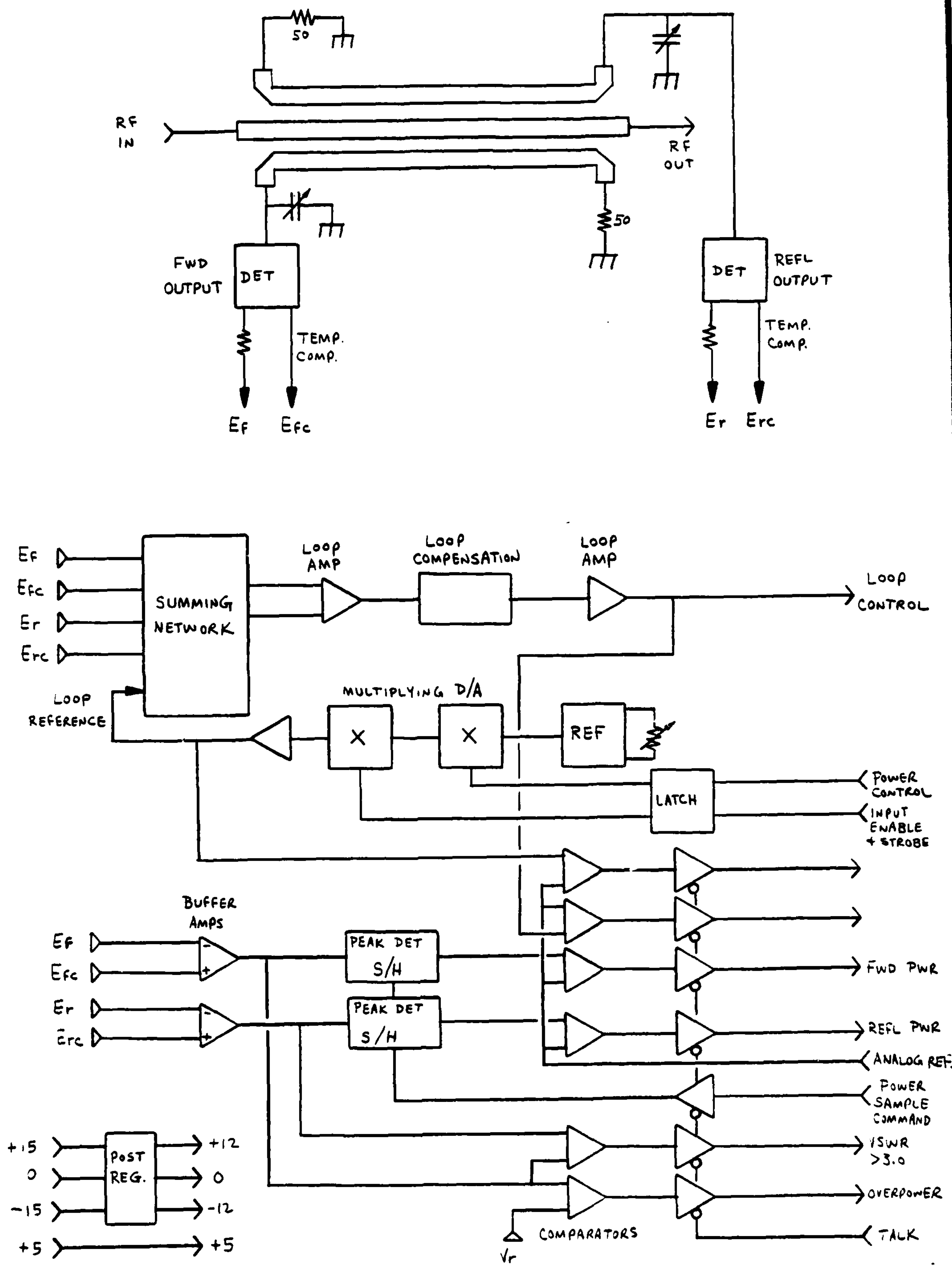


Figure 2.7-4 Coupler and Power Control Circuit

2.7.1 LOW PASS FILTER SUBASSEMBLY

The following specifications describe the low pass filter subassembly.

	MINIMUM	TYPICAL	MAXIMUM	UNITS
RF SPECIFICATIONS 30 - 88 MHz except as noted				
LOW BAND FILTER (See Figure 2.7-2)				
HIGH BAND FILTER (See Figure 2.7-3)				
FILTER INPUT SWITCH				
Switch Type		SPDT		
Input Power		650	750	Watts
Insertion Loss - To either output		0.1	0.15	dB
Isolation - To disabled path	30	35		dB
FILTER OUTPUT SWITCH				
Switch Type		SP3T		
Input Power				
Filter Ports		600	650	Watts
Bypass Ports		40	100	Watts
Insertion Loss - All paths		0.1	0.15	dB
Isolation - To both disabled ports	30	35		dB
ASSEMBLED UNIT				
Input Return Loss - Over band of selected filter	14	20		dB
Insertion Loss - Over band of selected filter		0.52	0.6	dB
- 2nd Harmonic	50			dB
- 3rd Harmonic	50			dB
- 4th Harmonic	60			dB
- To 3 GHz	60			dB

	MINIMUM	TYPICAL	MAXIMUM	UNITS
CONTROL INPUTS				
1. Filter Select				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = 30-52 MHz Filter			
	Logic 0 = 52-88 MHz Filter			
2. Amplifier Bypass				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Amplifier Bypass Enabled			
	Logic 0 = Power Amplifier Connected			
3. Output Select (Enables BITE Outputs)				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = High Impedance			
	Logic 0 = BITE Outputs Enabled			
BITE OUTPUTS[1]				
1. Low Band Filter Selected (Status of series diode bias)				
Protect Threshold		Normal Forward Bias		
Output Level		TTL Compatible		
Output Load			4	LS TTL
Sense	Logic 1 = Normal			
	Logic 0 = Failure			
2. High Band Filter Selected (Status of series diode bias)				
Protect Threshold		Normal Forward Bias		
Output Level		TTL Compatible		
Output Load			4	LS TTL
Sense	Logic 1 = Normal			
	Logic 0 = Failure			
3. Bypass Selected (Status of series diode bias)				
Signal Threshold		Normal Forward Bias		
Output Level		TTL Compatible		
Output Load			4	LS TTL
Sense	Logic 1 = Normal			
	Logic 0 = Failure			
4. High Voltage Present				
Signal Threshold	100		120	Volts
Output Level		TTL Compatible		
Output Load			4	LS TTL
Sense	Logic 1 = Normal			
	Logic 0 = Failure			

1 Outputs are Tri-State TTL and are enabled by OUTPUT SELECT line. All outputs are high impedance unless selected.

	MINIMUM	TYPICAL	MAXIMUM	UNITS
DC POWER SUPPLY INPUTS				
1. Logic Supply				
Voltage	4.75	5.0	5.25	Volts
Current		100	120	mAmps
2. PIN Diode Forward Bias				
Voltage	-6	-5	-4	Volts
Current		1.2	1.5	Amps
3. PIN Diode Reverse Bias Source				
Voltage	130	150	170	Volts
Current		0.5	1	mAmps

2.7.2 DIRECTIONAL COUPLER SUBASSEMBLY

The following specifications apply to the directional coupler subassembly.

	MINIMUM	TYPICAL	MAXIMUM	UNITS
RF SPECIFICATIONS 30 - 88 MHz except as noted				
INSERTION LOSS - THROUGH LINE		0.1	0.15	dB
THROUGH LINE IMPEDANCE		50		Ohms
COUPLED LINE IMPEDANCE		50		Ohms
COUPLING FACTOR				
Forward Power	32.8	33	34.2	dB
Reflected Power	32.8	33	34.2	dB
DIRECTIVITY				
Forward Line	26	30		dB
Reflected Line	26	30		dB
RF POWER LEVEL				
Forward		570	600	Watts
Reflected - Continuous			150	Watts
Reflected - 1 Second			600	Watts

COUPLED PORT LOAD
Adjustable shunt capacitor and full-wave detector (See 2.7.3)

2.7.3 CONTROL/PROTECT CIRCUIT SUBASSEMBLY

The following specifications define the control and protect circuits.

	MINIMUM	TYPICAL	MAXIMUM	UNITS
RF INPUTS (Directional Coupler Sample)				
1. Forward Power Sample		0.25	0.38	Watts
2. Reflected Power Sample			0.38	Watts
3. Source Impedance		50		Ohms
DETECTOR Full-wave rectifier with matching temperature compensation output on each RF input. Negative output voltage with applied power.				
1. DC Output Voltage Range (Differential)	-5		1	Volts
2. Compensation Voltage (Room Temperature)		0.25		Volts
3. Coupler/Detector Adjustment	-1.190	-1.200	-1.210	Volts
Set 1 capacitor and 1 variable resistor to specified value at 50 watts forward power at 30 and 88 MHz.				
4. Detector Load Impedance		1.8		kOhms

		MINIMUM	TYPICAL	MAXIMUM	UNITS
AMPLIFIER CONTROL LOOP					
1. Feedback Inputs					
Forward Voltage	(Ef)	-5		1	Volts
Forward Voltage Temperature Compensation	(Efc)		0.25		Volts
Reflected Voltage	(Er)	-5		1	Volts
Reflected Voltage Temperature Compensation	(Erc)		0.25		Volts
Load Impedance (All inputs)			1.8		kOhms

2. Control Equation -((Ef)-(Efc)) - 0.2 ((Er)-(Erc)) = Reference Voltage

	MINIMUM	TYPICAL	MAXIMUM	UNITS
3. Reference Generator				
DC Reference (Adjustable)	0		5	Volts

Frequency Multiplier: 0-1 multiplying factor to DC reference
8-bit latched binary input
TTL compatible input - 2 LSTTL loads max.

Power Control Multiplier: 0-1 multiplying factor to DC reference
8-bit latched binary input
TTL compatible input - 2 LSTTL loads max.

	MINIMUM	TYPICAL	MAXIMUM	UNITS
Reference Risetime		100		uS
4. Control Output				
Load Impedance		2		kohms
		100		pF
Range	-10		10	Volts
5. Control Loop Dynamics				
DC Gain	50	60	70	dB
Gain at 25 kHz	30			dB
Unity Gain Frequency		1		MHz

	MINIMUM	TYPICAL	MAXIMUM	UNITS
CONTROL SIGNAL OUTPUTS				
1. Forward Power				
Buffer Amplifier - Inverts detector output and compensation				
Peak Detecting Sample and Hold - Sample forward detector voltage				
Enable Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Hold Mode Logic 0 = Sample Mode			
Output Comparator - Compare S/H output to analog reference				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Voltage Exceeds Reference Logic 0 = Voltage Less Than Reference			
2. Reflected Power				
Buffer Amplifier - Inverts detector output and compensation				
Peak Detecting Sample and Hold - Sample reflected detector voltage				
Enable Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Hold Mode Logic 0 = Sample Mode			
Output Comparator - Compare S/H output to analog reference				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Voltage Less Than Reference Logic 0 = Voltage Exceeds Reference			
3. High VSWR (Signals VSWR greater than 3.0:1)				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = VSWR Less Than 3.0:1 Logic 0 = VSWR Exceeds 3.0:1			
4. Overpower (Signals output forward power greater than 575 watts)				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Normal Logic 0 = Output Exceeds 575 Watts			

	MINIMUM	TYPICAL	MAXIMUM	UNITS
CONTROL SIGNAL INPUTS				
1. Power Control Select Lines (2)				
Input 1 Frequency Control Word - Enables input latch to receive 8 bit power correction factor versus frequency.				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Normal Logic 0 = Enable Latch			
Input 2 Power Control Multiplier - Enables input latch to receive 8 bit correction factor for amplifier protection.				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Normal Logic 0 = Enable Latch			
2. Power Sample Command - Enables forward and reflected S/H circuits				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Hold Logic 0 = Sample			
3. Analog Reference Voltage				
Voltage	0		5	Volts
Load Impedance	20		33	kohms
			1000	pF
4. BITE/Control Signal Output Enable - Enables output signals				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Normal Logic 0 = Enable			
BITE OUTPUTS[1]				
1. Loop Reference (Signal Comparison Of Loop Reference Voltage To Analog Reference)				
Signal Threshold		0.0		Volts
Output Level		TTL Compatible		
Output Load			4	LS TTL
Sense	Logic 1 = Voltage Below Reference Logic 0 = Voltage Exceeds Reference			
2. Loop Output (Signal Comparison Of Loop Output Voltage To Analog Reference)				
Signal Threshold		0.0		Volts
Output Level		TTL Compatible		
Output Load			4	LS TTL
Sense	Logic 1 = Voltage Below Reference Logic 0 = Voltage Exceeds Reference			

1 Outputs are Tri-State TTL and are enabled by output select line. All outputs are high impedance unless selected.

	MINIMUM	TYPICAL	MAXIMUM	UNITS
DC POWER SUPPLY INPUTS				
1. Logic Supply				
Voltage	4.75	5.0	5.25	Volts
Current		100	150	mAmps
2. 15-Volt Control Supply				
Voltage	14	15	16	Volts
Current		50	75	mAmps
3. -15-Volt Control Supply				
Voltage	-16	-15	-14	Volts
Current		50	75	mAmps

2.8 RF INPUT PROCESSOR (A7)

After passing through the RF fail-safe mechanical relay assembly (A3), the RF input processor performs the initial modification of the characteristics of the input signal. The primary function of this module is to attenuate the wide-ranging input signal level to sub-bands at a maximum level compatible with the RF drive amplifier (A11) and to detect and count the frequency of the RF drive signal.

The driver signal is first passed through an electronic PIN diode switch assembly where it is routed to one of four paths, either the RF bypass to the amplifier output or to one of the three attenuator sections. A sample of the output signal is also routed through an attenuator and buffer amplifier to a frequency counter and level detector. The selected attenuator output is finally routed through an output switch and connected to the variable gain driver amplifier.

The input processor primarily functions to limit the drive level to the driver RF amplifier. Although the driver amplifier can withstand the highest expected input level, the full dynamic range of the system cannot be obtained with the amplifier attenuator alone. The input processor switches one of two fixed attenuators or, at low drive levels, a through connection into the input RF path according to the drive level present. The selected attenuator is normally the highest attenuation, but is reduced to a lower level by the processor if the full output is not acheived after a short time delay. After switching to a lower level, that level is maintained as long as power is applied unless the input suddenly increases. A hardware reset increases attenuation when drive levels increase beyond the desired level. Control signals feed back the selected attenuation in addition to the frequency and input level to the power amplifier system control processor.

The input processor is mounted inside the power amplifier case in an inclosed plug-in module. Because of the power dissipation with high driver power levels, a substantial heat sink is used to move the heat to the case heat exchanger.

Electrical specifications for the input processor are contained in the following section and Figure 2.8-1 contains a functional block diagram of the module.

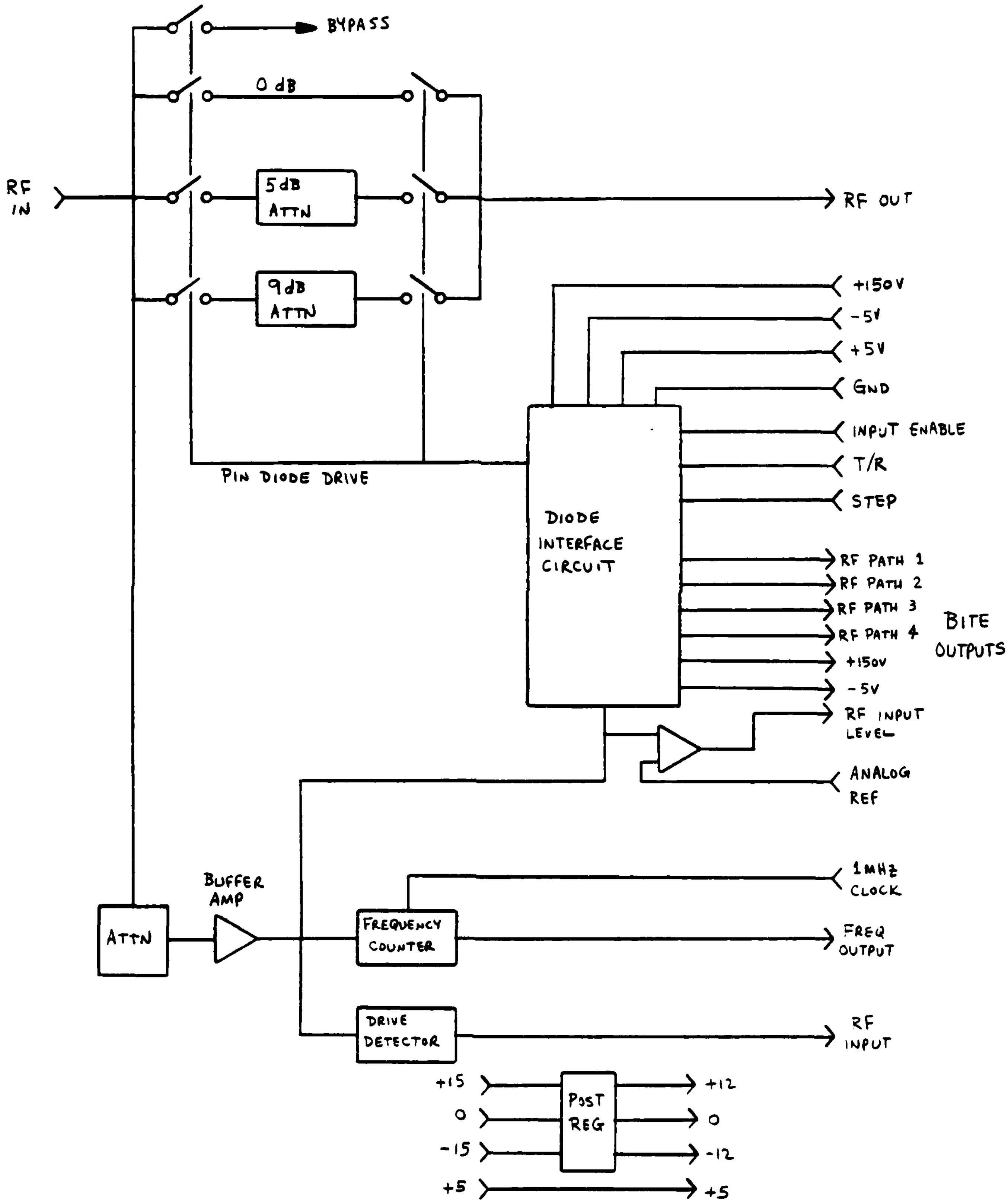


Figure 2.8-1 RF Input Attenuator and Processor

2.8.1 RF INPUT PROCESSOR SPECIFICATIONS

Electrical specifications describing the function of the RF input processor module are listed in this section.

	MINIMUM	TYPICAL	MAXIMUM	UNITS
RF INPUT				
1. Power Level	3.0	40	100	Watts
2. Input Impedance		50		Ohms
3. Input VSWR				
Input over 15 watts			1.5	
Input under 15 watts		1.5	2.0	
RF OUTPUT POWER	2.8		12	Watts
FREQUENCY COUNTER				
1. Input Sensitivity		27	30	dBm
2. Resolution		1		MHz
3. Clock Input		1		MHz
4. Update Period			2	uSec
5. Counter Signal Isolation to RF Input	60			dB
6. Output		8 bit Binary Word TTL Compatible		
RF INPUT DETECTOR				
1. Detector Threshold		23	26	dBm
2. Signal Output				
Level		TTL Compatible		
Load			6	LS TTL
Sense	Logic 1 = No Signal Applied Logic 0 = RF Input Present			

	MINIMUM	TYPICAL	MAXIMUM	UNITS
RF ATTENUATOR				
1. Attenuation Levels		0		dB
		5		dB
		9		dB
2. Attenuator Switch		PIN Diode Configuration		
Insertion Loss/Section		0.1	0.15	dB
Switching Time			25	uSec
3. Input Bypass				
Insertion Loss		0.1	0.15	dB
Off Isolation	25	30		dB
CONTROL INPUTS				
1. Attenuator Select - Determines selected input attenuator				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = No Change			
	Logic 0 = Reduce Attenuation 1 Step			
2. Bypass Select				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Amplifier Connected			
	Logic 0 = Bypass			
3. Input Enable - Enables input transceiver for control commands				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Normal			
	Logic 0 = Input enabled			
4. Counter Output Select				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = High impedance output			
	Logic 0 = Output frequency word			
5. BITE Output Select				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = High impedance output			
	Logic 0 = Output BITE status			
6. Analog Reference Voltage				
Voltage	0		5	Volts
Load Impedance	20		33	kohms
			1000	pF

	MINIMUM	TYPICAL	MAXIMUM	UNITS
CONTROL/BITE OUTPUTS				
1. Amplifier Bypass Selected				
Level		TTL Compatible		
Load			6	LS TTL
Sense	Logic 1 = False Logic 0 = Bypass Active			
2. Attenuator = 0 dB				
Level		TTL Compatible		
Load			6	LS TTL
Sense	Logic 1 = False Logic 0 = 0 dB Active			
3. Attenuator = 5 dB				
Level		TTL Compatible		
Load			6	LS TTL
Sense	Logic 1 = False Logic 0 = 5 dB Active			
4. Attenuator = 9 dB				
Level		TTL Compatible		
Load			6	LS TTL
Sense	Logic 1 = False Logic 0 = 9 dB Active			
5. 150-Volt Supply				
Level		TTL Compatible		
Load			6	LS TTL
Sense	Logic 1 = Normal Logic 0 = Failure			
6. -5-Volt Supply				
Level		TTL Compatible		
Load			6	LS TTL
Sense	Logic 1 = Normal Logic 0 = Failure			
7. -12-Volt Supply				
Level		TTL Compatible		
Load			6	LS TTL
Sense	Logic 1 = Normal Logic 0 = Failure			
8. RF Input Level (Comparison Of Detected Input To Analog Reference)				
Signal Threshold		0.0		Volts
Level		TTL Compatible		
Load			6	LS TTL
Sense	Logic 1 = Voltage Below Reference Logic 0 = Voltage Exceeds Reference			

	MINIMUM	TYPICAL	MAXIMUM	UNITS
DC POWER SUPPLY INPUTS				
1. Logic Supply				
Voltage	4.75	5.0	5.25	Volts
Current		150	200	mAmps
2. PIN Diode Forward Bias				
Voltage	-6	-5	-4	Volts
Current		1.2	1.5	Amps
3. PIN Diode Reverse Bias Source				
Voltage	130	150	170	Volts
Current		0.5	1	mAmps
4. 15-Volt Control Supply				
Voltage	14	15	16	Volts
Current		20	50	mAmps
5. -15-Volt Control Supply				
Voltage	-16	-15	-14	Volts
Current		20	50	mAmps

2.9 SPLITTER - SIX-WAY (A8)

The six-way RF power splitter is a passive device that divides the output of the RF driver amplifier into six equal parts to uniformly drive the six paralleled RF output amplifiers. The splitter is matched to the combiner (A9) such that the driver amplifier power is split and summed in amplitude and phase to minimize RF losses. In addition, isolation between output ports is required to minimize interaction between amplifiers (to avoid potential feedback conditions) and to reduce the input VSWR in the event of an output RF amplifier failure. Balance between outputs insures equal sharing of the output load between amplifiers.

The power splitter consists of an impedance transformation circuit and a power splitter that essentially divides the output of the low impedance common summing node to the six 50-ohm output ports while maintaining a good input impedance match. Ballast resistors provide output isolation in the event of an output amplifier failure by effectively replacing a portion of the failed output load. In normal operation, the voltage at all outputs is identical, resulting in no loss in the resistors. Low loss ferrites are used in the transformer and divider to minimize shunting currents in the transmission line shields and insure proper voltage division.

Since the power splitter contains no active circuits, no explicit BITE circuits are included. A failure in this module will be identified as no output from any of the six output amplifiers when the driver amplifier is active or as no output from a known-good single output amplifier. Both conditions should be identifiable from a visual inspection as a failed connection.

The key design objectives for this module are low insertion loss and uniform power division.

Electrical specifications for the power splitter are listed in the following section. Figure 2.9-1 is a block diagram of the six-way splitter.

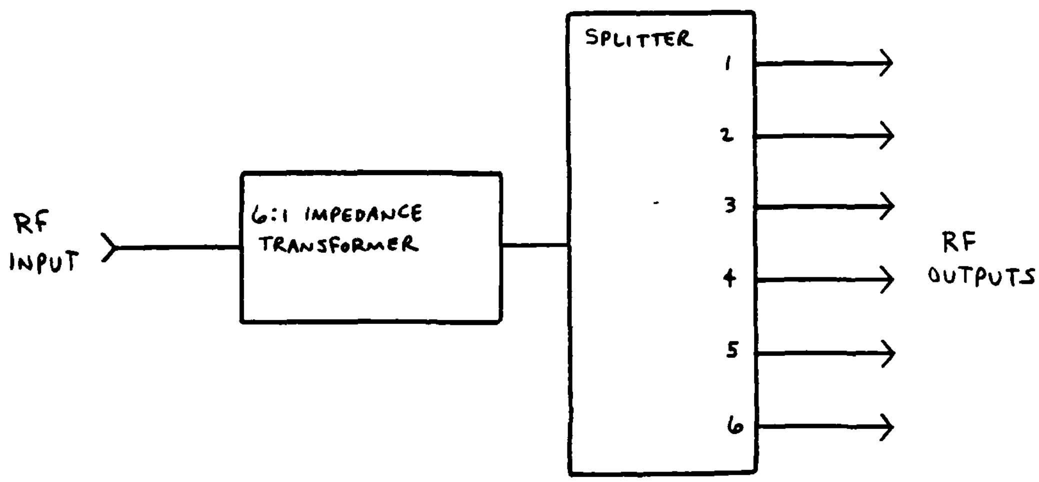


Figure 2.9-1 Six-way RF Power Splitter Block Diagram

2.9.1 POWER SPLITTER DESIGN REQUIREMENTS

Electrical characteristics of the six-way power splitter are listed below.

FREQUENCY RANGE 30 - 88 MHz

NUMBER OF OUTPUT PORTS 6

	MINIMUM	TYPICAL	MAXIMUM	UNITS
INPUT FORWARD POWER		65	80	Watts
INSERTION LOSS		0.2	0.35	dB
INPUT/OUTPUT IMPEDANCE		50		Ohms
INPUT RETURN LOSS	14	20		dB
OUTPUT AMPLITUDE BALANCE		0.2	0.25	dB
OUTPUT PORT ISOLATION	15	20		dB
DUMP RESISTORS		35 20		Ohms Watts

CONNECTORS

Input SMA Series

Output SMA Series

2.10 COMBINER - SIX-WAY (A9)

The six-way RF power combiner is a passive device used to sum the outputs of the six RF power output amplifiers to a common 50-ohm output line. The combiner is essentially a mirror image to the power splitter and is designed to handle much higher power levels. Because of the output power required from this module, significant effort is necessary to minimize losses and guarantee adequate voltage breakdown capability.

Section 2.9 contains a general description of the operation of the power combiner. The following section lists the electrical requirements of the module, and Figure 2.10-1 is a block diagram of the unit.

2.10.1 POWER COMBINER DESIGN REQUIREMENTS

Electrical specifications for the RF power combiner are listed below.

FREQUENCY RANGE 30 - 88 MHz

NUMBER OF INPUT PORTS 6

	MINIMUM	TYPICAL	MAXIMUM	UNITS
OUTPUT FORWARD POWER		650	750	Watts
INSERTION LOSS		0.2	0.35	dB
INPUT/OUTPUT IMPEDANCE		50		Ohms
INPUT RETURN LOSS (Each Port)	14	20		dB
AMPLITUDE BALANCE		0.2	0.25	dB
INPUT PORT ISOLATION	15	20		dB
DUMP RESISTORS		35		Ohms
		250		Watts

CONNECTORS

Input	TNC Series
Output	TNC Series

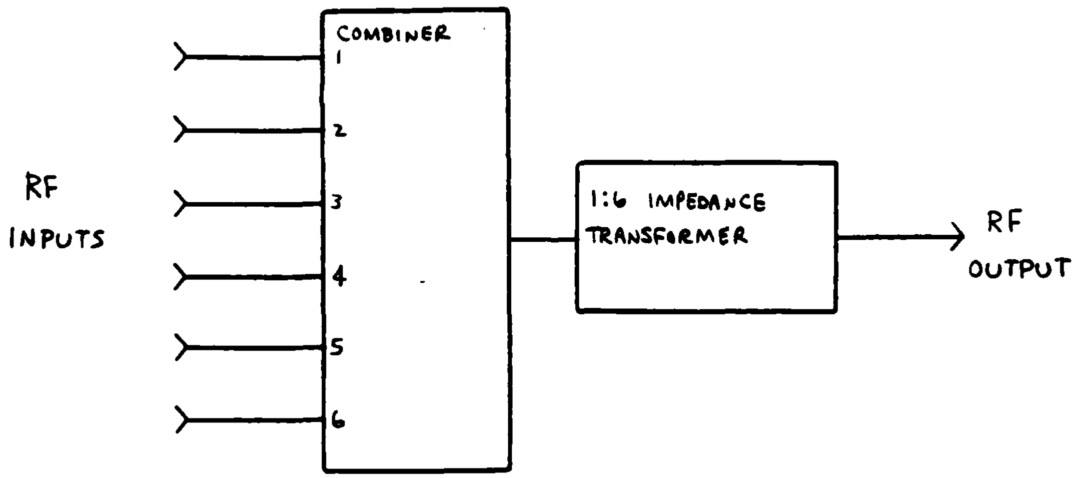


Figure 2.10-1 Six-way RF Power Combiner Block Diagram

2.11 POWER SUPPLY - DRIVER AMPLIFIER (A10)

The driver amplifier power supply is a switching regulator to provide primary power voltages to the companion RF driver amplifier (A11) and isolate the amplifier from the vehicular supply (See Appendix A.3). The switching converter is synchronized to an external clock and is operated 180 degrees out-of-phase from a similar input level control circuit power supply to reduce conducted switching emissions. Further, the input source lines are totally isolated from the equipment case to minimize chassis currents. A separate ground-referenced control circuit power source is provided by the control circuit power supply (A5) to operate the supply controller.

Several BITE outputs are generated in the supply to permit monitoring by the system controller (A2) of both the power supply and the RF driver amplifier operation. BITE outputs include over- and undervoltage sense and a foldback current limit circuit and output level indicator.

Because of the high efficiency of the switching regulator, this assembly is mounted within the equipment case. To minimize EMI exposure to the output lines, the module is located adjacent to the load (A11).

Electrical specifications for the power converter assembly are listed in the following section. Figure 2.11-1 is a block diagram of the power converter.

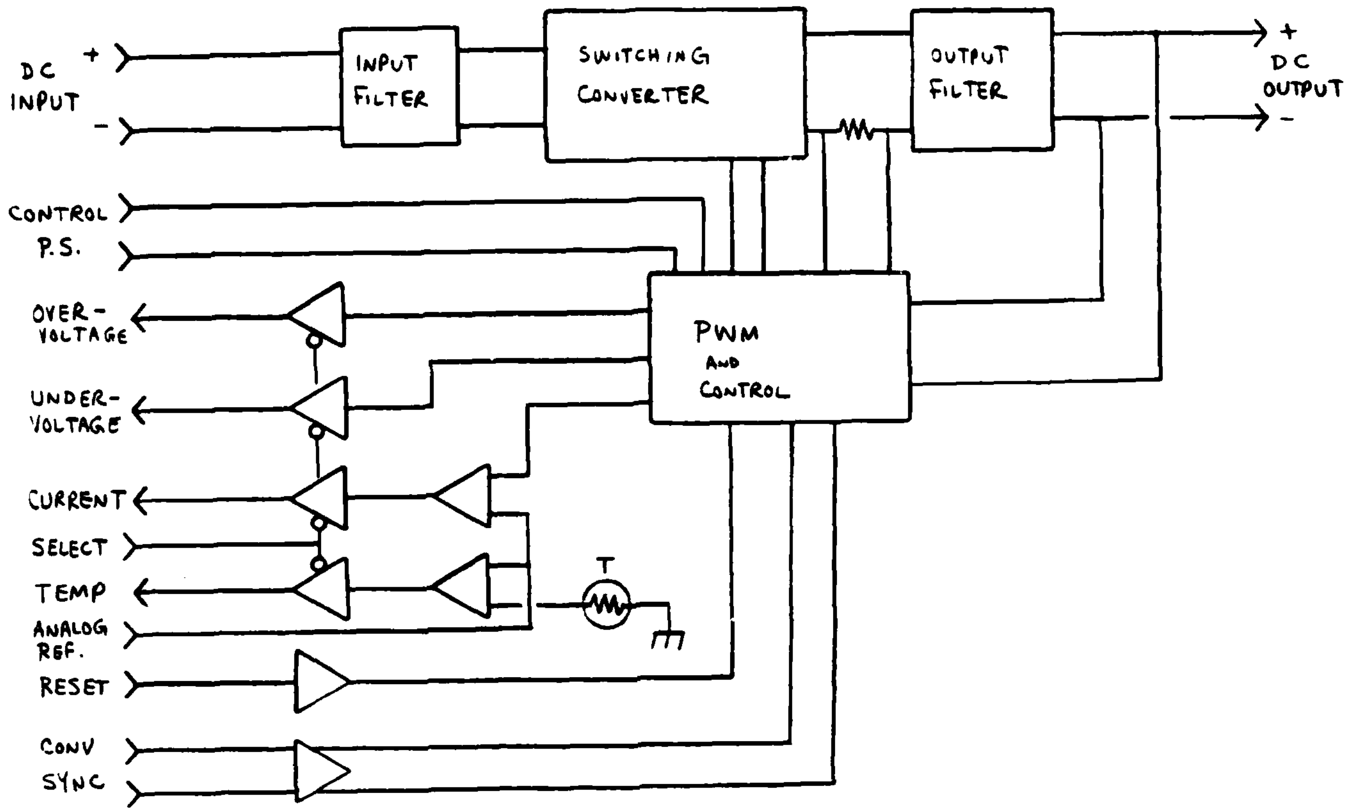


Figure 2.11-1 Driver Amplifier Power Supply

2.11.1 DRIVER AMPLIFIER POWER SUPPLY REQUIREMENTS

The following specifications describe the power supply assembly.

CONFIGURATION	Switching, coupled-inductor current-driven buck converter.
SWITCHING FREQUENCY	100 kHz

	MINIMUM	TYPICAL	MAXIMUM	UNITS
DC OUTPUTS				
1. Amplifier DC Supply				
DC Voltage	26.5	28.0	29.5	Volts
Ripple (Components to 1 MHz)			-20	dB
Ripple (Components above 1 MHz)			-90	dB
DC Current	0	4.2	5.0	Amps

NOTE: Current reduces linearly by approximately 0.4 dB/volt for input voltages below 27.5 volts. See Figure 2.1-4. Supply to include current limit circuit to fold-back at loads above 5.0 amps.

	MINIMUM	TYPICAL	MAXIMUM	UNITS
DC INPUTS				
1. *Primary Power Source*[1]				
Differential DC Voltage	21.5	27.0	32	Volts
Ripple Voltage (50 Hz-200 kHz)			14	Volts pk-pk
DC Input Current			6.5	Amps
Supply Efficiency	80	83		Percent

1 Input voltage per MIL-STD-1275A (See Appendix A.3).
Voltage at supply processed by input circuits and EMI filter (A4 and A1FL1).
Input DC circuit to be totally DC isolated from case ground.

	MINIMUM	TYPICAL	MAXIMUM	UNITS
2. Switching Converter Control Source				
DC Voltage (Ground Referenced)	8	12	15	Volts
Input Current			150	mAmps

	MINIMUM	TYPICAL	MAXIMUM	UNITS
CONTROL INPUTS				
1. Clock (Converter Sync)				
Frequency	180	200	220	kHz
Duty Cycle	9	10	11	Percent
Level		TTL Compatible		
Load			2	LS TTL
2. Analog Reference (Output Current Measurement)				
Voltage	0		5	Volts
Load Impedance	20		33	kohms
			1000	pF
Conversion Factor	1.45	1.5	1.55	Amps/Volt
3. Output Select (Enables BITE Outputs)				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = High Impedance			
	Logic 0 = BITE Outputs Enabled			
4. Supply Reset (Permits Recovery Attempt From Auto-Shutdown)				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Normal			
	Logic 0 = Reset			
BITE OUTPUTS[1]				
1. Overvoltage (Signal Overvoltage Protect)				
Protect Threshold			30.0	Volts
Output Level			TTL Compatible	
Output Load			4	LS TTL
Sense	Logic 1 = Normal			
	Logic 0 = Protect			
2. Undervoltage (Signal Undervoltage Protect)				
Protect Threshold	26.0			Volts
Output Level			TTL Compatible	
Output Load			4	LS TTL
Sense	Logic 1 = Normal			
	Logic 0 = Protect			
3. Current (Signal Comparison To Analog Reference)				
Signal Threshold		0.0		Volts
Output Level			TTL Compatible	
Output Load			4	LS TTL
Sense	Logic 1 = Current Below Reference			
	Logic 0 = Current Exceeds Reference			

1 Outputs are Tri-State TTL and are enabled by OUTPUT SELECT line. All outputs are high impedance unless selected.

2.12 RF DRIVER AMPLIFIER ASSEMBLY (A11)

The driver RF amplifier assembly amplifies the attenuated RF input signal to a level sufficient to drive the six combined RF output amplifiers. Although this amplifier is similar in design to the output amplifier, there are several key differences in design requirements. First, the amplifier and corresponding power supply are separated because of packaging volume constraints. As with the output amplifiers, the driver must also perform into high load VSWRs. However, because this amplifier drives the output amplifier modules, which are deliberately mismatched to obtain improved gain flatness versus frequency, the driver must be capable of operating into a high load VSWR at the low frequency end of the band under normal conditions without obtaining a power reduction to reduce stresses. The driver amplifier is also designed using smaller transistors to obtain higher gain to permit operation with low-level transmitters and to obtain lower capacitive feedback to minimize VSWR-induced oscillatons. Finally, the driver amplifier contains the variable-gain element of the power control feedback loop.

Amplifier protection and BITE is provided via the driver amplifier power supply (A10). This protection function is achieved by limiting available primary power to the amplifier transistors. BITE is obtained by checking that the amplifier is drawing DC current when driven. Because the driver amplifier is a single line in the amplifier chain (no redundancy), reliability of this module is essential to operation of the power amplifier. All parts are significantly derated to extend reliability. The paralleled amplifiers also reduce the stresses on each individual amplifier.

The RF driver amplifier assembles directly to a plug-in finned heat exchanger mounted to the rear of the equipment case. All heat-producing parts are fastened directly to the heatsink to obtain maximum cooling efficiency. Key design factors to reduce heat are to maximize gain and efficiency while maintaining ruggedness to operate under the conditions described.

Electrical specifications for the driver RF amplifier assembly are provided in the following section. Figure 2.12-1 contains a block diagram of the driver amplifier.

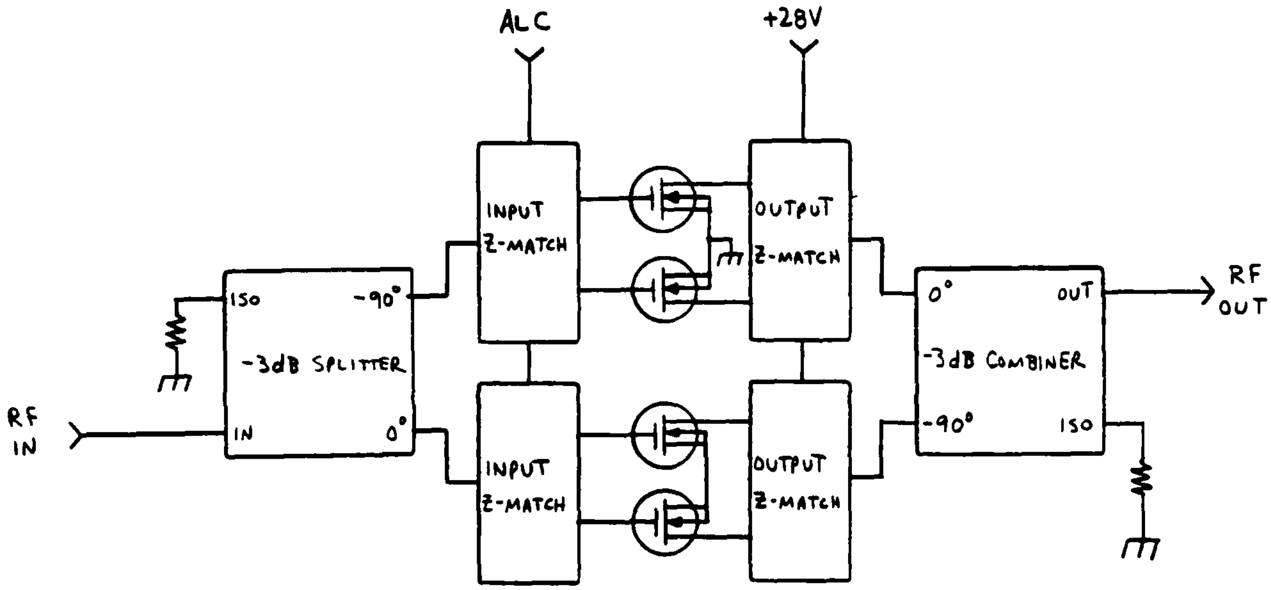


Figure 2.12-1 RF Driver Amplifier Block Diagram

2.12.1 RF DRIVER AMPLIFIER ASSEMBLY REQUIREMENTS

The following specifications describe the RF driver amplifier.

CONFIGURATION	Quadrature-Combined, Variable Gain, Push-Pull, Class AB Biased RF Amplifiers
RF TRANSISTORS	Two 80-watt, 175 MHz, Field-Effect Parts
FREQUENCY RANGE	30 - 88 MHz

RF OUTPUT

1. Nominal Forward Power — 65 Watts Maximum

NOTE: The driver amplifier sees the load VSWR of the combined RF output amplifier assembly plus the translated antenna (load) VSWR on a continuous basis. At low frequencies where driver amplifier load VSWR is poor, output amplifier gain is high to compensate for saturation. Linearity must be maintained and damage may not occur under any load VSWR condition with continuous drive applied. DC input current is limited to 5 amps under all conditions.

2. Harmonics

NUMBER	MAX. LEVEL (dBc)
2	-20
3	-10
4	-30
Higher	-30

3. Spurious Outputs — -100 dBc max. greater than 1 MHz from the carrier.

RF GAIN

LOAD VSWR = 1.0 BIAS = 10 Volts

FREQUENCY (MHz)	MIN. GAIN (dB)	MAX. GAIN (dB)
30	15	22
88	14	18

GAIN CONTROL CHARACTERISTICS

1. Dynamic Range (12 Watts RF Input)
   - 30 MHz — 23 dB Minimum
   - 88 MHz — 17 dB Minimum

2. RF Input Power Range — 2.5 to 12 Watts Continuous; 100 Watts Maximum - 1 Second

3. Input Impedance — 2 kOhms; 100 pF

4. Control Voltage Range — -10 to 10 Volts

RF INPUT MATCH

LOAD VSWR = 1.0

FREQUENCY (MHz)	MIN. RETURN LOSS (dB)
30	-15
88	-15

DC INPUT POWER

	MINIMUM	TYPICAL	MAXIMUM	UNITS
1. Amplifier DC Supply				
DC Voltage	26.5	28.0	29.5	Volts
Ripple (Components to 1 MHz)			-20	dB
Ripple (Components above 1 MHz)			-90	dB
2. Efficiency-Current (Output = 65 Watts, Load VSWR = 1.0, 30-88 MHz)				
Output Efficiency	50	55	75	Percent
Current		4.2	4.6	Amps

BITE

No explicit BITE outputs available. BITE via corresponding power supply output current.

CONNECTORS

1. RF Input and Output — Automatic PMMA Series

2. DC and Control — AMP Modu Series

2.13 RF OUTPUT AMPLIFIER (A12 - A17)

The RF output amplifier assembly provides the gain and output power capability to overcome losses in the output circuits and achieve the 500-watt output level required. This assembly must be capable of operating into the load VSWR of the antenna system, which at VHF is relatively uncontrolled and typically ranges up to 5:1. Since the amplifier is to be used in a moving vehicle, the load will vary with time and position of the vehicle. Further, the amplifier module includes an integral power supply regulator to isolate the RF amplifier from the widely-varying vehicular supply (See Appendix A.3) and to provide the required voltages for the amplifier and its bias source.

Six output amplifiers are paralleled to achieve the required power output. A combiner and splitter provide the necessary isolation between amplifiers and also phase-stagger the load impedance seen by each amplifier. Therefore, when operating into high load VSWR's, amplifiers saturated because of the load presented are compensated by the other amplifiers of the set, and the full required output is obtained. The switching power supplies are also phase-staggered to reduce switching transients at the power amplifier input and reduce conducted emissions.

Reduction of amplifier module stresses resulting from operation at extreme conditions is provided via integral protection circuits and from the monitor and control functions of the system processor assembly (A2). Internal functions include supply shut-down in response to over- or undervoltage conditions and a current limit circuit to limit the available power to the RF amplifier transistors when operating into high-current load VSWR phases. Protection conditions are signalled to the system controller for further response as required. The processor acts to reduce output power in response to out-of-range input voltages, high load VSWR, excessive temperature, circuit failures, etc. All parts are significantly derated to extend reliability.

All output amplifiers are identical in design and construction and are mounted directly to finned heat sinks assembled about the equipment case periphery to obtain maximum cooling. Because the unit is convection cooled, the RF amplifier and power supply subassemblies are designed for maximum efficiency and gain to minimize heat dissipation.

Electrical specifications for the output amplifier subassemblies are listed in the following sections. Figure 2.13-1 contains a block diagram of the output amplifier.

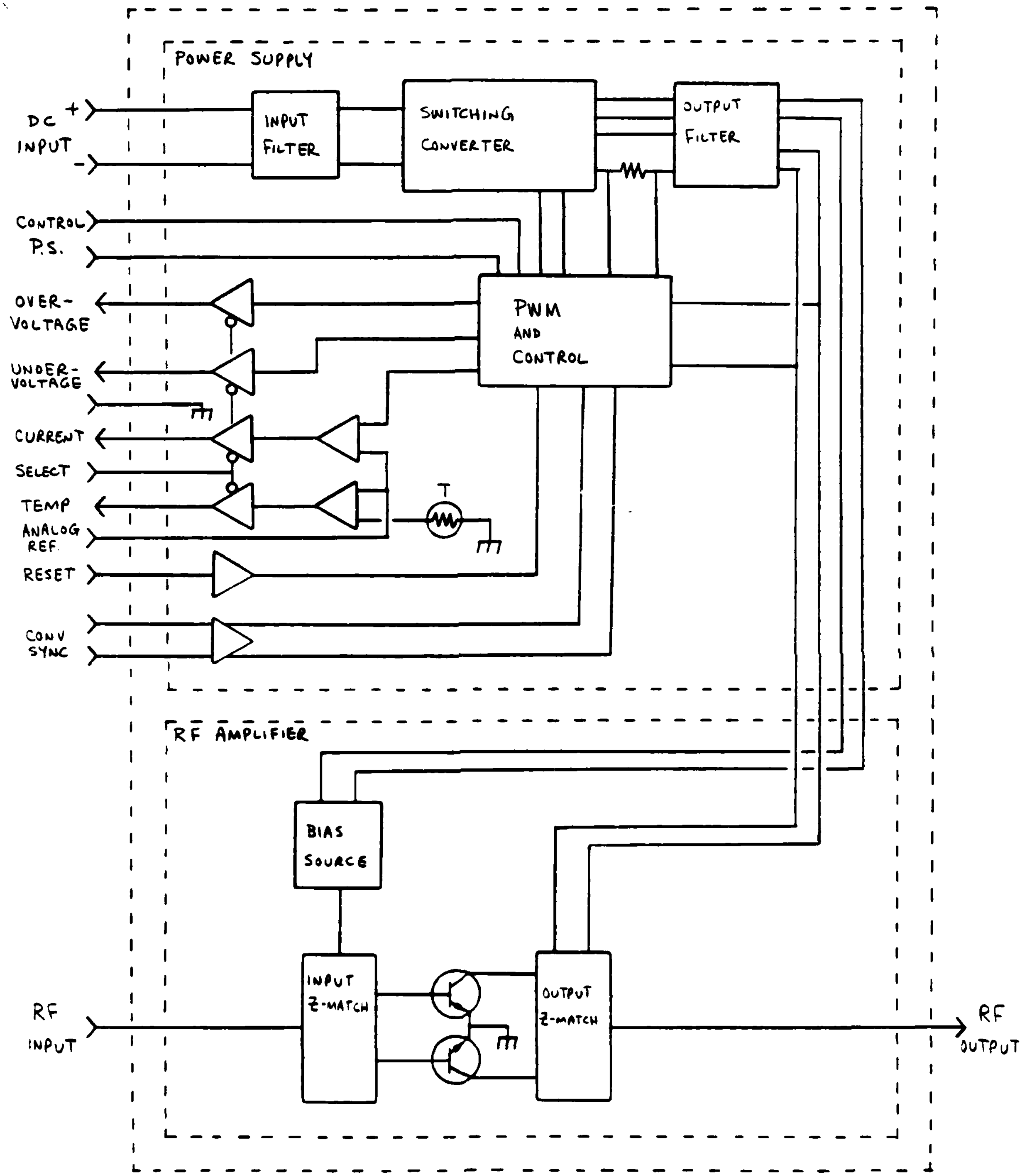


Figure 2.13-1 RF Output Amplifier Assembly

2.13.1 RF POWER AMPLIFIER SUBASSEMBLY REQUIREMENTS

The following specifications describe the RF power amplifier.

CONFIGURATION	Push-Pull, Class AB Biased RF Amplifier
RF TRANSISTORS	Two 100-watt, 175 MHz, Bipolar Parts
FREQUENCY RANGE	30 - 88 MHz

RF OUTPUT

1. Nominal Forward Power

MAX. POWER (W)	LOAD VSWR	TIME
125	1.0	Continuous
105	3.0	Continuous
100	5.0	1 Second
70	5.0	Continuous
95	10.0	1 Second
50	10.0	Continuous
90	Infinite	1 Second
32	Infinite	Continuous

NOTE: RF drive will be present to attempt to achieve listed short-term output. Saturation of the amplifier under this condition is acceptable, but damage must not occur. Listed power into VSWR is 1/6 of total output requirement and assumes equal load sharing. DC input current will be limited to 9 amps under all conditions.

2. Harmonics

NUMBER	MAX. LEVEL (dBc)
2	-20
3	-10
4	-30
Higher	-30

3. Spurious Outputs -100 dBc max. greater than 1 MHz from the carrier.

RF GAIN

LOAD VSWR = 1.0

FREQUENCY (MHz)	MIN. GAIN (dB)	MAX. GAIN (dB)
30	12	18
88	11.25	15

RF INPUT MATCH

LOAD VSWR = 1.0

FREQUENCY (MHz)	MIN. RETURN LOSS (dB)
30	-2
88	-10

DC INPUT POWER

	MINIMUM	TYPICAL	MAXIMUM	UNITS
1. Amplifier DC Supply				
DC Voltage	26.5	28.0	29.5	Volts
Ripple (Components to 1 MHz)			-20	dB
Ripple (Components above 1 MHz)			-90	dB
2. Bias Source Supply				
DC Voltage	3.6	4.0	4.4	Volts
Ripple (Components to 1 MHz)			-20	dB
Ripple (Components above 1 MHz)			-60	dB
3. Efficiency-Current (Output = 125 Watts, Load VSWR = 1.0, 30-88 MHz)				
Output Efficiency	55	60	75	Percent
Current				
Amplifier		7.5	8.1	Amps
Bias Source	0.1	0.3	0.9	Amps
4. Bias Source Output				
Output Voltage[1] (25°C)	0.3		0.55	Volts
Spurious Content			-90	dB

1 Adjust with a select-at-test resistor to voltage greater than 0.3 VDC that corresponds to 11.5 dB minimum RF gain at 88 MHz with a maximum voltage limit of 0.55 VDC.

BITE

No explicit BITE outputs available. BITE via integrated power supply output current.

CONNECTORS

1. RF Input and Output — Automatic PMMA Series

2. DC and Control — AMP Modu Series

2.13.2 POWER SUPPLY SUBASSEMBLY REQUIREMENTS

The following specifications describe the power supoly subassembly.

CONFIGURATION	Switching, coupled-inductor current-driven buck converter.
SWITCHING FREQUENCY	100 kHz

	MINIMUM	TYPICAL	MAXIMUM	UNITS
DC OUTPUTS				
1. Amplifier DC Supply				
DC Voltage	26.5	28.0	29.5	Volts
Ripple (Components to 1 MHz)			-20	dB
Ripple (Components above 1 MHz)			-90	dB
DC Current	0	7.5	9.0	Amps

NOTE: Current reduces linearly by approximately 0.4 dB/volt for input voltages below 27.5 volts. See Figure 2.1-4. Supply to include current limit circuit to fold-back at loads above 9.0 amps.

	MINIMUM	TYPICAL	MAXIMUM	UNITS
2. Bias Source Supply				
DC Voltage	3.6	4.0	4.4	Volts
Ripple (Components to 1 MHz)			-20	dB
Ripple (Components above 1 MHz)			-60	dB
DC Current	0.01	0.3	0.9	Amps

NOTE: Bias source load is directly proportional to the output supply load.

	MINIMUM	TYPICAL	MAXIMUM	UNITS
DC INPUTS				
1. Primary Power Source[1]				
Differential DC Voltage	21.5	27.0	32	Volts
Ripple Voltage (50 Hz-200 kHz)			14	Volts pk-pk
DC Input Current			11.75	Amps
Supply Efficiency - 9 Amps	78	80		Percent
- 7.7 Amps	80	83		Percent

1 Input voltage per MIL-STD-1275A (See Appendix A.3).
Voltage at supply processed by input circuits and EMI filter (A4 and A1FL1).
Input DC circuit to be totally DC isolated from case ground.

	MINIMUM	TYPICAL	MAXIMUM	UNITS
2. Switching Converter Control Source				
DC Voltage (Ground Referenced)	8	12	15	Volts
Input Current			150	mAmps

	MINIMUM	TYPICAL	MAXIMUM	UNITS
CONTROL INPUTS				
1. Clock (Converter Sync)				
Frequency	180	200	220	kHz
Duty Cycle	10	12.5	50	Percent
Level		TTL Compatible		
Load			2	LS TTL
2. Analog Reference (Output Current Measurement)				
Voltage	0		5	Volts
Load Impedance	20		33	kohms
			1000	pF
Conversion Factor	2.9	3.0	3.1	Amps/Volt
3. Output Select (Enables BITE Outputs)				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = High Impedance			
	Logic 0 = BITE Outputs Enabled			
4. Supply Reset (Permits Recovery Attempt From Auto-Shutdown)				
Level		TTL Compatible		
Load			2	LS TTL
Sense	Logic 1 = Normal			
	Logic 0 = Reset			
BITE OUTPUTS[1]				
1. Overvoltage (Signal Overvoltage Protect)				
Protect Threshold			30.0	Volts
Output Level			TTL Compatible	
Output Load			4	LS TTL
Sense	Logic 1 = Normal			
	Logic 0 = Protect			
2. Undervoltage (Signal Undervoltage Protect)				
Protect Threshold	26.0			Volts
Output Level			TTL Compatible	
Output Load			4	LS TTL
Sense	Logic 1 = Normal			
	Logic 0 = Protect			
3. Current (Signal Comparison To Analog Reference)				
Signal Threshold		0.0		Volts
Output Level			TTL Compatible	
Output Load			4	LS TTL
Sense	Logic 1 = Current Below Reference			
	Logic 0 = Current Exceeds Reference			

1 Outputs are Tri-State TTL and are enabled by OUTPUT SELECT line. All outputs are high impedance unless selected.

3.0 RESULTS

The amplifier module specifications and design characteristics described in Section 2 establish a basis for the detailed design and function of the individual amplifier modules. When completed, the compliant individual modules will permit the desired performance goals for the 500-watt amplifier to be acheived.

In addition to the system definition for the power amplifier, a number of contractual data items have been completed and submitted during the first quarterly reporting period. This data includes:

- Radioactive Material Report
- Nomenclature Request
- Nameplate Request
- Preliminary Reliability Prediction
- Electromagnetic Inteference Control Plan

A program kick-off meeting was held with CECOM technical and contract personnel on 12 October 1982. During this meeting a number of design modifications and potential problem areas were discussed. Major issues and preliminary oral resolutions are listed below.

- RF Input Connector. A change to type "BNC" connectors on the RF input was discussed to make the amplifier compatible with the RF output connector used on the RT-246 (VRC-12) and SINCGARS radios. A recommendation was made to keep the originally-specified type "N" connector based on MIL-STD-461 RE02 radiated emissions requirements and the poor leakage performance of the type "BNC" connectors. The present design connector is as originally specified.

- Power Control Switch. A request to add a switch enabling the operator to select a lower output level was made, with a level of 250-watts suggested. The current design approach includes this switch.

- Right Angle DC Power Connector. Because of the length of the DC power cable and connector extension beyond the amplifier chassis, a consideration of adapting the input connector to a right angle configuation was made. Subsequent analysis of the cost impact and the discovery of the true flexibility of the cable have resulted in this issue being abandoned.

- Manual Keying. A request to eliminate manual keying was made based on the lack of a tactical use of this feature and the fact that the amplifier response in automatic key mode would be the default mode of operation when manually keyed to avoid output power overshoot resulting from keying the amplifier before RF drive was applied. Problems with Problems with the automatic frequency counter - filter select circuit function which unkeys the amplifier in response to frequency changes to prevent damage caused by driving the incorrect low pass filter were also explained. This characteristic prohibits the use of wide range swept input signals with the amplifier. The present design eliminates the manual key operating mode and input circuits.

- Power Connectors. Potential vehicle problems with handling the amplifier primary supply current using the specified connector were discussed. A specification error in the connector stuffing tube Federal Stock Number was also corrected. CECOM engineers have investigated the connector rating problem and decided that the specified part will perform as intended. The equipment power cable will be terminated at the vehicle end with the specified connector.

The amplifier specification, CENCOMS 31-88 dated 2 March 1981 reproduced in Appendix A.1 has been modified to incorporate the verbally-discussed modifications. Formal notification of these changes has still not been received at this time.

The following government-furnished property has been received to be used in support of the amplifier testing phase of the development program:

- 2 Transceivers RT-246/VRC
- 2 Handsets H-250/U
- 2 Technical Manuals TM 5820-401-34-2

Two power connectors, GCU-3444/VRC, are still outstanding.

Finally, a relatively large number of electrical parts orders has been placed for long-lead and firm-design components. Although some parts are promised beyond the desired delivery dates, no particular problems have been encountered that cannot be worked-around at this time. Purchase orders will continue to be monitored, especially on devices requiring special burn-in screening, to insure that deliveries are met. Purchasing and component selection efforts are continuing.

4.0 FUTURE EFFORT

During the next reporting period, refinement of the next level of detail of the amplifier design will be accomplished. The design of the system controller software and BITE isolation procedures will also begin. This effort will include a study of the system timing and response periods to external effects.

Fabrication of the initial parts for the deliverable advanced development models is scheduled along with continued procurement of electrical parts for the amplifier modules. Documentation efforts for the amplifier design will also begin in the next reporting period.

APPENDIX A.1

CENCOMS 31-88 AMPLIFIER SPECIFICATION

CENCOMS 33-81
2 March 1981

CORADCOM
TECHNICAL REQUIREMENTS

500 WATT SOLID-STATE RF POWER AMPLIFIER

1. SCOPE

1.1 This advanced development specification applies to the fabrication and testing of a 500 Watt, solid-state efficient, broad-band power amplifier covering the frequency range of 30 to 88 MHz.

2. APPLICABLE DOCUMENTS

2.1 Issue of documents. The following documents of the issue in effect on the date of invitation for bids, form a part of this specification to the extent specified herein:

STANDARDS

MILITARY

MIL-S-901 C (1)	Shock test (High Impact) Shipboard Machinery, Equipment and Systems, Requirements for, 5 Sep 63
MIL-P-11268	Parts, Materials and Processes used in Electronic Equipment 31 Aug 78
MIL-M-13231A(3)	Marking of Electronic Items, 11 Nov 71
MIL-F-14072 (B)	Finishes for Ground Signal Equipment, 19Apr76
MIL-STD-252 B	Wired Equipment, Classification of Visual and Mechanical Defects, 19 Jan 70
MIL-STD-454 G	Standard General Requirements for Electronic Equipment, 15 Mar 80
MIL-STD-810 C	Environmental Test Methods for Aerospace and Ground Equipment, 10 Mar 75
MIL-STD-1275 A	Characteristics of 28 Volt DC Electrical Systems in Military Vehicles, 17 Sep 76

MIL-STD-1472(B)	Human Engineering Design Criteria for Military Systems, Equipment and Facilities, 31 Dec 74
MIL-E-52835A (2)	Enamel, Modified Alkyd, Camouflage Lusterless, 22 May 80
Code of Federal Regulations Title 29 Chapter XVII, Part 1910	Occupational Safety and Health Standards
MIL Hdbk 217	Reliability Prediction of Electronic Equipment 9 Apr 79
MIL-STD-461X B	Electromagnetic Emission and Susceptibility, Requirements for the Control of EMI., 1 Apr 80
MIL-I-23053/X 3A(1)	Insulation Sleeving, Electrical, Heat Shrinkable, Polyoefin, Flexible Crosslinked , 19 Oct 79
MIL-STD-462	Measurement of EMI Characteristics 31 Jul 67

3. REQUIREMENTS

3.1 Engineering objective. A rugged amplifier that can be built from established state-of-the-art technology in solid state. RF high power amplifiers in the VHF frequency range.

3.2 Development objectives:

a. A power amplifier which can be used to increase the transmitter power level (40 watt nominal) of Army tactical FM radios.

b. High efficiency resulting in a dc current drain compatible with internal vehicular power supplies.

c. Minimum size commensurate with performance requirements and reasonable cost.

d. Capable of interfacing with ... the RT-524A/VRC or future SINCGARS-V radio in an automatic PTT operation.

e. Shall be primarily employed in vehicular mounted (M577 type) configurations.

3.3 Design considerations

3.3.1 Frequency range. 30 to 88 MHz. The specified range shall be covered in not more than three (3) frequency bands, which can be manually selected by the operator. Within each frequency band, there shall be no tuning required by the operator when changing the operating frequency.

3.3.2 Supply voltage. 27.5V dc nominal. 22-32V dc range and transients per MIL-STD-1275.

3.3.3 System impedance level. The system input and output impedance levels shall be 50 ohms, nominal.

3.3.4 Input drive power. 40W nominal. With an Input VSWR of 2:1, the available power from the drive source is reduced by not more than 1 dB from the nominal.

3.3.5 Output power. For a drive power as specified in 3.3.4, the variation in the output forward power (referenced to the nominal 500 watts) shall not exceed the limits given below.

Tolerance in the output forward power variation (dB)	Supply Voltage (Volt DC)	Load VSWR
+2, -0	27.5	1
+2, -1	27.5	3.0
+1, -2.5	22	1

An output power level switch shall be provided to reduce the power 3 dB from the nominal levels listed above.

3.3.6 Maximum current drain. The maximum current drain from the vehicular power supply shall not exceed 80A in all operating conditions specified herein.

3.3.7 Duty cycle. The amplifier shall be capable of continuous 1.0 minute on and 1.0 minute off operation, with a goal of continued 30 minutes on and 30 minutes off.

3.3.8 Damage protection. The equipment shall be protected against reverse supply voltage connection. Thermal protection shall be provided against both inadvertent continuous duty operation of the amplifier, and operation under restricted ventilation.

3.3.8.1 Protection against infinite VSWR. No permanent damage shall occur to the equipment if it is keyed continuously into an infinite load VSWR of any phase at any frequency within the operating band.

3.3.8.2 Hot switching protection. The equipment shall be protected from any damage against inadvertent switching from one frequency band to another while in transmission of rf.

3.3.8.3 Out-of-band drive portection. The equipment shall be protected against any damage when driven by a full nominal drive and: a. The drive frequency is out of the selected band frequency but within the 30-88 MHz range.

3.3.8.4 In-band overdrive protection. The equipment shall be protected against any damage when driven by an input, within the 30-88 MHz band, greater than the nominal rating by up to a maximum of 3 dB.

3.3.8.5 Vehicular supply protection. The equipment shall have a fuse or circuit breaker in its power ON/OFF line to disconnect the power from the vehicle to the equipment in the event of equipment malfunction (i.e. short circuit). This safety feature must insure protection to the vehicular power supply.

3.3.9 Keying Control. Automatic keying controls shall be provided. The keying control shall place the amplifier either in transmit or receive mode. In the receive mode, the amplifier is by-passed between the RF input and output connectors with a minimum insertion loss.

3.3.9.1 Automatic Mode. In the automatic mode no operator handling, other than primary power "ON/OFF", shall be necessary. The amplifier keying shall be controlled by the RF input drive. The automatic keying shall not present infinite VSWR load to the driver while the RF drive is present. The maximum amount of time allowable between presence of 50% of nominal RF drive and full power-up of the amplifier shall not exceed 50 milliseconds.

3.3.10 Bite. The equipment shall provide a means of self-testing. This self-test shall be used to monitor equipment performance and perform preliminary diagnosis. Bite shall be able to be conducted without having to dismantle any part of the equipment.

3.3.11 Cables/Connectors/Switches. The equipment shall have cables and connectors as set forth below:

3.3.11.1 ON/OFF Switch. The equipment shall have a manual primary power ON/OFF switch on the front panel.

3.3.11.2 RF connectors. The equipment shall have type "N" rf connectors for input and output of rf signals.

3.3.11.3 Power cable and connector. The equipment shall be provided with the following power cable/connector.

a. The power cable shall be approximately 12 feet long. One end shall have a "Bendix" Connector Assembly which is composed of a Connector, Plug, Electrical (Bendix) FSN 5935-856-8426 and an Adapter (Bendix) Stuffing Tube (½ in) FSN 5935-892-8931. This cable end shall mate with the power receptacle on the vehicle. No other system function shall be included in this cable/connector combination.

3.3.12. Physical characteristics. The equipment shall conform to the physical specification set forth below.

3.3.12.1 Size. The volume and depth dimension of the equipment shall be as follows:

a. Volume = 2200 cubic inches maximum.

b. Depth = 14 inches maximum

3.3.12.2 Weight. The equipment shall have a maximum weight of no more than 75 lbs.

3.4 Nuclear survivability. DELETED

3.5 Environmental Conditions.

3.5.1 Temperature.

a. High temperature.

(1) Operating. The equipment shall be operable without degradation in specified performance at ambient air temperature as high as 125°F (+51.7°C).

(2) Storage and transportation. The equipment shall withstand exposure to ambient air temperatures as high as +160°F (+71°C).

b. Low temperature.

(1) Operating. The equipment shall be operable without degradation in specified performance as ambient temperatures as low as -60°F (-50°C).

(2) Storage and transportation. The equipment shall withstand exposure to ambient air temperatures as low as -70°F (-56°C).

3.5.2 Humidity. The equipment shall be operable without degradation in specified performances and shall sustain no physical damage, during and after prolonged exposure to extreme high humidity levels as encountered in tropical areas.

3.5.3 Explosive atmosphere. The equipment shall not cause ignition of an ambient-explosive-gaseous mixture with air when operating in such an atmosphere.

3.5.4 Vibration. The equipment shall withstand vibration and shock induced during field transport by military vehicle and/or as part of a vehicular installation over all types of roads and cross country terrain. The equipment shall also withstand shock encountered during rough handling and servicing. The equipment installed within or upon an armored vehicle shall be resistant to high level shock caused by ballistic impact, air blast explosions and similar combat field conditions.

3.5.5 Immersion. The equipment shall be capable of being immersed to a covering depth of 3 feet of water.

3.6 Electromagnetic interference.

3.6.1 Electromagnetic emission and susceptibility. The amplifier, when operating and performing its intended functions, shall comply with the following requirements of MIL-STD-461B.

CE01	CS01	RE02 (a)	RS03 (c)
CE03 (a)	CS02		
CE06 (b)	CS06		

a. Conducted and radiated switching transients shall comply with MIL-STD-461B limits specified in figure 4-4 and paragraph 15.2.2 respectively.

b. Spurious emissions shall be held 100dB below the carrier.

c. The field strength levels and Modulation characteristics for RS03 shall be as follows:

Freq. Range (Hz)	"E" field V/M	Mod. Characteristics
10K-2M	1	AM, 50%, 1 kHz tone
2M-30M	5	AM, 50%, 1 kHz tone
30M-76M	10	FM, 8 kHz Dev., 1 kHz tone
76M-400M	10	AM, 50%, 1 kHz tone
400M-2G	10	Pulse 0.1 microsec., 400 PPS
2G-10G	5	Pulse 0.1 microsec., 400 PPS

3.6.2 Bonding and grounding. The amplifier shall be designed with adequate provisions for bonding the unit. The bonding shall not be accomplished through the screws that are used to mount the unit. Shock mounts or vibration isolators, if employed, shall utilize bonding straps to bypass the mounts or isolators. Bonding jumpers, when used, shall be of the solid metal type and shall be as short as possible with length to width ratios not exceeding 5 to 1. The surfaces being bonded together shall be free of all high impedance elements. The impedance between a single metal-to-metal mating surface shall not exceed 2.5 milliohms. Upon completion of the bonding assembly and ascertainment of the specified bonding impedance and the completed assembly shall be refinished with the original finish or other protective finish in accordance with MIL-F-14072.

3.6.3 Cables and connectors. Coaxial cables shall be of the double shielded type. The cables shall have their shields terminated in connectors with EMI backshell to provide peripheral bonding of the shields. The connector shell shall be free of nonconductive finishes and provide positive bonding and grounding with mating connectors and the unit chassis ground. The impedance between a single mating connection shall not exceed 2.5 milliohms.

3.7 Reliability. The reliability design goal for the 500 watt power amplifier shall be a mean-time-between failure of 4800 hours. Achievement of this requirement shall be verified by a detailed stress analysis reliability prediction per MIL HDBK-217.

3.8 Parts, materials and processes. Electronic component parts, devices, materials, techniques and technologies, including micro-electronics, shall conform to MIL-P-11268.

3.9 Markings. Markings shall conform to MIL-M-13231.

3.10 Colors. Colors shall be lusterless green in accordance with MIL-F-14072 and MIL-E-52835A.

3.11 Finish. Finishes shall be in accordance with MIL-F-14072.

3.12 Workmanship. Workmanship shall be in accordance with requirement 9 of MIL-STD-454.

3.13 Safety engineering. The equipment design criteria shall be in accordance with Title 29, Code of Federal Regulations, Chapter XVII, Part 1910, "Occupational Safety and Health Standards," Requirement 1, MIL-STD-454; and paragraphs entitled "Labeling" and "Hazards and Safety" of MIL-STD-1472, and shall include but not be limited to the following:

3.13.1 Personnel safety. The system shall be designed to minimize the probability and severity of injury to personnel throughout the systems life cycle. Personnel safety is an absolute requirement of the equipment and shall not be considered a candidate for trade-off.

3.13.1.1 Mechanical safety. The system design shall include the safety provisions called for in paragraph entitled "Mechanical" of Requirement 1, MIL-STD-454 and the following:

a. Exposed edges shall be rounded to a minimum radius of 0.04 inch (1 mm), and exposed corners to a minimum of 0.5 inch (12.7 mm).

b. Adequate provisions for lifting and handling shall be provided in accordance with paragraph entitled "Unit Design for Efficient Handling," MIL-STD-1472.

c. Adequate safeguards shall be installed to prevent inadvertant entrapment of body parts and clothing in moving parts.

d. Color coding of indicator lights shall conform with Table II, MIL-STD-1472.

3.13.1.2 Electrical safety. The system design shall include the provisions called for in paragraph entitled "Electrical" of Requirement 1, MIL-STD-454 and the following:

a. Accidental contact with current-carrying metal components, terminals, and like devices (greater than 70 volts) shall be controlled by the following:

(1) Wire connections (bare terminals) shall be protected with insulated sleeving (MIL-I-23053/5).

(2) All contacts, terminals, and like devices other than wire connections shall be provided with barriers or guards to prevent operating and maintenance personnel from accidental contact. These barriers or guards shall be manufactured from a transparent, nonconductive material (insulation resistance shall be not less than 1000 megohms) and shall be marked with the approximate highest voltage (nearest round number) and current type which may be encountered upon removal. The marking shall be in a format in accordance with American National Standards Institute (ANSI) Z35.1-1972 and worded as follows: "CAUTION (Maximum Voltage applicable) Volts AC." (or DC when applicable).

(3) Small openings shall be provided (where needed) in guards or barriers for maintenance testing without the removal of the guards. The voltage encountered through these openings shall be marked on the guard or barrier.

b. Components over 500 volts shall be completely inclosed and interlocked with no bypass devices permitted and shall be marked in accordance with paragraph entitled, "Warning Markings," Requirement 1, MIL-STD-454.

c. Socket connectors, designed to prevent personnel from accidental contact with potentially hazardous voltage, shall be used on electrically energized contacts such as power sources.

d. When radio interference filters are used in the power input, filters shall contain only capacitors between each side of the line and chassis which are sufficiently low in value to allow less than 5 milliamperes of current to flow to the chassis under the most adverse conditions of maximum power frequency and maximum voltage permitted by the individual test equipment specification.

e. Positive acting, automatically actuated discharging devices shall be provided to discharge high voltage circuits and capacitors to 30 volts within 2 seconds or less.

f. Attachment plugs shall have dead-front construction per 1979 NEC Article 410-56(d).

3.13.1.3 Chemical safety. The system design shall include the following provisions:

a. No material or component which during any phase of the life cycle will evolve toxic gases, vapors, fumes, or droplets shall be used in the system.

b. No treating materials shall be used that are identified in the Toxic Substance List (published by National Institute for Occupational Safety and Health) that will produce toxic effects via the respiratory tract, eye, skin (cutaneous and subcutaneous), or mouth. This includes handling the treated material during fabrication, transportation, operation or maintenance of the parts in which the treated materials are used or during use of the finished parts when used for the purpose intended.

3.13.2 Equipment Safety.

a. The system shall be designed to minimize equipment damage, degradation of efficiency or mission failure due to the following conditions:

(1) Operator induced errors

(2) Improper cabling

(3) Power failure or electrical overstress on components.

(4) Secondary failures

(5) Installation, storage, operation, handling, maintenance, and transportation.

b. Specific design techniques for equipment protection shall include the following:

(1) Electrical overload protection shall be in accordance with Requirement 8, MIL-STD-454. All fuse positions shall be marked with the rated current capacity of the fuse to be employed therein. Fuse positions for delayed-action fuses shall have the additional designation "SLOW". For "bayonet" type fuses, the contract nearest the insertion end shall be at ground potential when the fuse is removed.

(2) Positive means shall be provided to prevent the inadvertent reversing or mismating of instrument leads and electrical connections.

3.13.3 Environmental safety.

No radioactive material shall be utilized without prior express approval of the Contracting Officer (potential sources of radiation include luminous dials/markings, electron tubes, surge arrestors and lenses).

3.14 The contractor shall provide drawings for identification plates (data item A001), Nomenclature Request (A002), Level 1 Drawings (A003), Operation/Maintenance Manual (B001), Scientific and Quarterly reports (C001, C002, C003) and Presentation Material (G001) .

3.15 Repair and Maintenance

The contractor shall accomplish fault identification and effect repairs to restore to operational capability to 500W RF Power Amplifier units being utilized in Development and Operational testing (DT/OT1) on an on-call basis during the test period. The contractor shall have a cognizant technical representative with the necessary equipment and materials on-call during this test period to provide these services. The contractor must have technical personnel at the designated area within 24 hours after receipt of the oral notification.

3.16 Refurbishment

Immediately following DT/OT1, the equipment shall be returned to the contractor's plant for refurbishment, the extent of which will be determined at that time, after which the equipment will be sent to Fort Monmouth, NJ for Final Acceptance.

4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for inspection. Unless otherwise specified in the contract or purchase order, the contractor is responsible for the performance of all inspection and test requirements as specified herein. Likewise, the contractor may use his own or any other facilities suitable for the performance of the inspection and test requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform any of the inspections and tests set forth in the specification where such inspections and tests are deemed necessary. Test equipment and facilities for Government tests and inspection shall be made available by the contractor. The Government reserves the right for authorized technical representatives to witness any contractor performed inspections and/or tests.

4.2 Inspection covered by susbidiary documents. The following shall be inspected under the applicable subsidiary documents as part of the inspections required by this specification.

Item	Where Required
Parts, Materials and Processes	3.8
Marking	3.9
Colors	3.10
Finish	3.11

4.3 Visual and mechanical inspection. Equipments shall be examined for defects in compliance with MIL-STD-252. This inspection shall be performed to determine compliance with 3.12.

4.4 Quality conformance inspection of equipment before preparation for delivery. The contractor, to demonstrate compliance with specified requirements, shall perform the inspections and tests specified in 4.2, 4.3, 4.5, 4.6 and 4.7 of this specification. This does not relieve the contractor of his responsibility for performing any additional inspections and/or tests, which are deemed necessary to control the quality of the product and to assure that all requirements are met for all specified functions and at all frequencies within the specified tuning range. The contractor shall make available, for Government review, inspection and test procedures, inspection and test records and test data. Test data shall be prepared for eqch equipment tested by the contractor or his agents. The data shall present the exact results of measurements made or readings observed and shall be expressed in the same terms as expressed by the requirements. Check marks, "X," ditto marks or statements that requirements were met, will not be construed as necessary data unless approved in advance by the Government.

In addition, the Government at its discretion and without notice elsewhere in the contract may perform inspections and/or tests independent of the inspections and/or tests required to be performed by the contractor. Such inspections and/or tests shall be for all or any part of the specified inspections/tests to verify the contractor's compliance with specified requirements. Test equipment to be used by Government respresentatives for such tests shall be made available by the contractor. Further, all facilities and services necessary for the placement, operation and maintenance of these test equipments shall be provided by the contractor.

4.5 Electrical tests. Electrical tests shall be performed in accordance with a contractor prepared, Government approved test plan.

4.6 Environmental tests. Environmental tests shall be performed in accordance with the Government approved test plan and the requirement of paragraphs 4.6.1 through 4.6.7 of this specification.

4.6.1 Temperature.

4.6.1.1 High temperature. The equipment shall be subjected to the test of Method 501.1, Procedure II, of MIL-STD-810. For Step 7, the chamber temperature shall be adjusted to 51.7°C (-70°F). Low operating temperature (Step 4) shall be -51°C (-60°F).

4.6.2 Humidity. The equipment shall be subjected to the test of Method 507.1 of MIL-STD-810, Procedure II or III depending on the design of the equipment. Procedure III shall be used if the equipment contains areas normally sealed during operation by gasket or other non-heremetic type seal. In Step 7 of Procedure III, the chassis shall be removed from its enclosure or the test item shall be otherwise opened so as to expose the normally sealed areas to the chamber environment. In Step 6 of either procedure, measurements shall be taken during the last 5 hours of the last cycle.

4.6.3 Vibration and shock.

4.6.3.1 Vibration.

a. Part I. The equipment in its transit case, if any, shall be subjected to Method 514.2, Procedure XI, Part 2 of MIL-STD-810. Operate the test item and record performance electrical test measurements. Inspect the test item mechanically.

b. Part II. The equipment shall be subjected to the test of Method 514.2, Procedure VIII, Category f, Curve W of Figure 514.2-6 of MIL-STD-810. The time schedules shall be in accordance with Table 514.2-VI. At the conclusion of the above test, visually inspect the test item for any evidence of mechanical damage and operate the test item and compare the results with pre-preformance test data.

4.6.3.2 Shock. The equipment shall be subjected to the tests of Method 516.2, Procedure II and V of MIL-STD-810. Equipments to be installed in or upon armored type vehicle shall be subjected to the test of MIL-S-901 for Type A, Lightweight equipment. Mounting of the equipment on the test plate shall simulate the most severe condition which may be encountered in service.

4.6.4 Immersion. The equipment shall be subjected to the test of Method 512.1, Procedure I, of MIL-STD-810. This test shall be performed prior to and following vibration and shock testing of the same test item.

4.6.5 Explosive atmosphere (armored vehicle) environment. The equipment shall be subjected to the test of Method 511.1, Procedure I, of MIL-STD-810.

4.7 Electromagnetic interference.

4.7.1 Electromagnetic Interference. The amplifier shall be tested for compliance with the requirements of 3.6.1. Test procedures shall be in accordance with the test methods of MIL-STD-462, Notice 3. A test plan must be prepared by the contractor and submitted to the Government for approval prior to EMI testing.

4.7.1.1 Bonding and Grounding. Prior to performing the EMI tests of 4.7.1 compliance with the bonding requirements of 3.6.2 and 3.6.3 shall be ascertained. The bonding impedance shall be measured and the data recorded in the EMI test report.

4.8 System Safety

4.8.1 Safety evaluation. A safety evaluation shall be conducted by the contractor to determine that all personnel, equipment, and environmental hazards have been identified and eliminated, in compliance with 3.13.

4.8.2 Safety Inspection. During acceptance inspection, a visual inspection shall be performed to determine that all requirements, as a result of the safety evaluation, have been incorporated in the equipment. Inability to meet the requirements of 3.13 shall constitute a failure of the test.

4.9 Acceptance. Acceptance shall be based on the contractor's fulfillment of the requirements of section 3 and the delivery and acceptance of all items listed in section 4.

4.9.1 Preliminary Quality Assurance (PQA) - Preliminary testing, inspection and acceptance shall be conducted in accordance with the Government approved -contractor written test plan.(E001)

4.9.2 (NONE)

4.9.3 Final Acceptance. Final acceptance will be conducted at Fort Monmouth, after equipment has been refurbished at contractor's plant, following OTI. Final Acceptance inspections and tests will consist of the following: sections 3.9, 3.10, and 3.11 of this document and ON/OFF test, BITE, RF Power Out vs. RF Power In and Frequency and RF Power out vs DL Power In and Frequency.

5.0 Development Testing/Operational Testing 1 (DT/OT1). The equipment shall be submitted to a DT/OT1 stage after preliminary acceptance has taken place.

5.1 Development Testing 1. Development testing will be the responsibility of the Government. The Government reserves the right, if so desired, to use the Preliminary Assurance Test as the Development test. If additional DT is requred the location will be determined at that time. The contractor shall be provided with a copy of the test plan, at least thirty (30) days prior to start of test to review and comment.

5.2 Operational Test 1. Operational Testing will be conducted immediately following Development Testing. The Government will be responsible for the Operational Testing. The contractor shall be provided with a copy of the operational test plans, at least 30 days prior to start of test to review and comment.

5. PACKAGING

5.1 Equipment shall be packed and marked appropriately to prevent damage during shipment.

6. NOTES

APPENDIX A.2

MIL-STD-461B SUMMARY

APPENDIX A.2

MIL-STD-461B SUMMARY

A.2.1 INTRODUCTION

The following paragraphs summarize key requirements of MIL-STD-461B for elecromagnetic compatibility as related to the design of the 500-watt VHF power amplifier.

A.2.2 CE01 - CONDUCTED EMISSIONS, POWER AND INTERCONNECTING LEADS, LOW FREQUENCY (30 Hz to 15 kHz)

Emissions from DC supply leads to the amplifier are controlled. Limits are established in Figure A.2-1, Curve 1 when measured in a 75 Hz effective bandwidth.

A.2.3 CE03 - CONDUCTED EMISSIONS, POWER AND INTERCONNECTING LEADS, 15 kHz TO 50 MHz

CE03 is applicable to DC supply leads to the amplifier. Limits are established in Figure A.2-2, Curve 1 for narrowband emissions and Figure A.2-3, Curve 1 for broadband emissions.

Key narrowband frequencies and limits for the VHF amplifier are:

FREQUENCY (kHz)	LIMIT (dBuA)	LIMIT (uA)
200	51	355
400	42	126
600	36	63
800	32	40
1000	29	28

A.2.4 CE06 - CONDUCTED EMISSIONS, ANTENNA TERMINALS, 10 kHz TO 3 GHz

This requirement limits spurious and harmonic signals at the antenna terminals. Limits do not apply within +/- 5 percent of the carrier frequency.

Conducted emissions limits are:

1. Key-up or standby mode		
Narrowband	34 dBuV	(-73 dBm in 50 ohms)
Broadband	40 dBuV/MHz	(-67 dBm/MHz in 50 ohms)
2. Harmonics		
2nd and 3rd	-67 dBc	
4th and up	-80 dBc	
3. Spurious Signals		
All	-100 dBc	

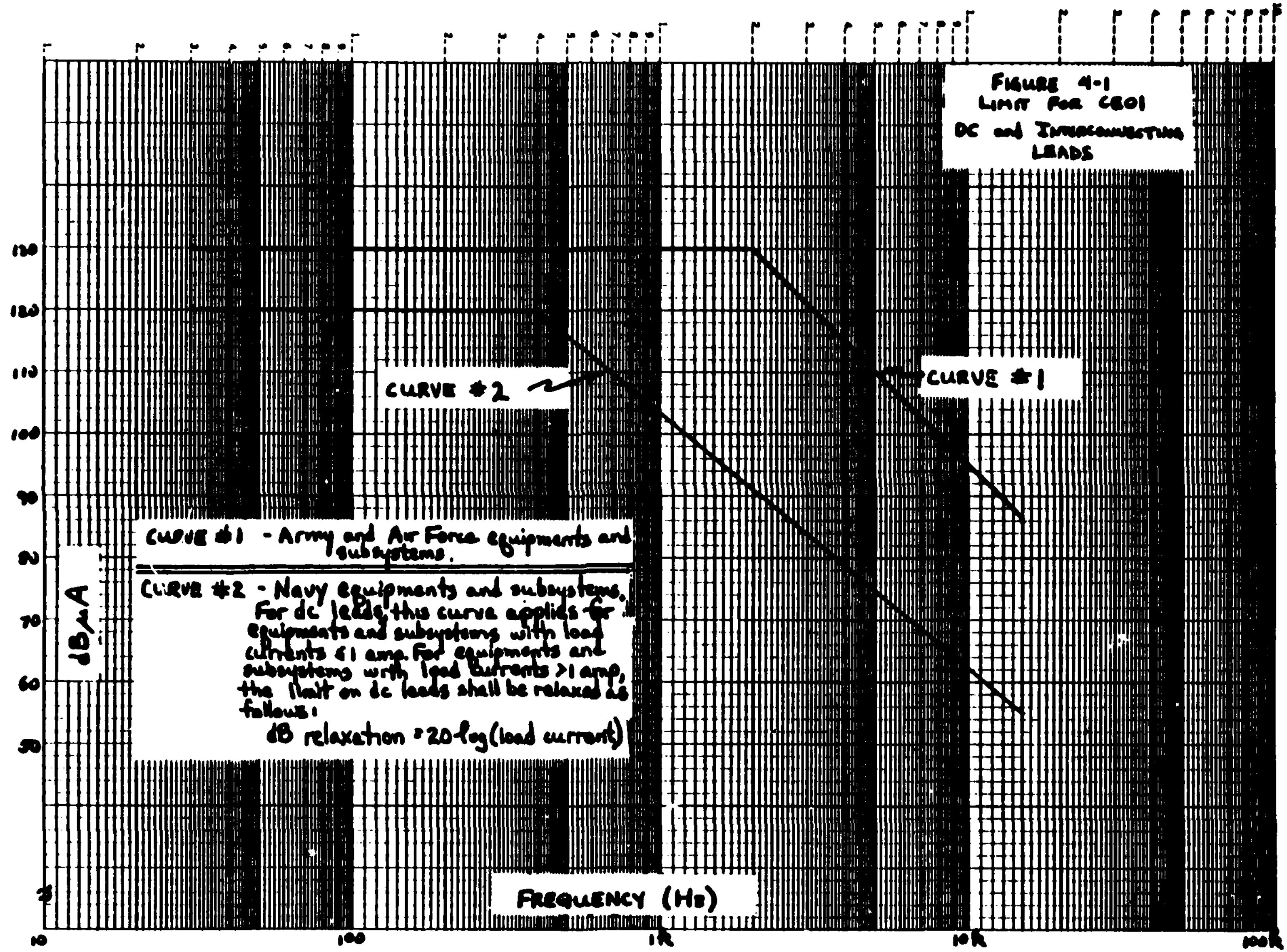


Figure A.2-1 LIMIT FOR CE01 DC AND INTERCONNECTING LEADS

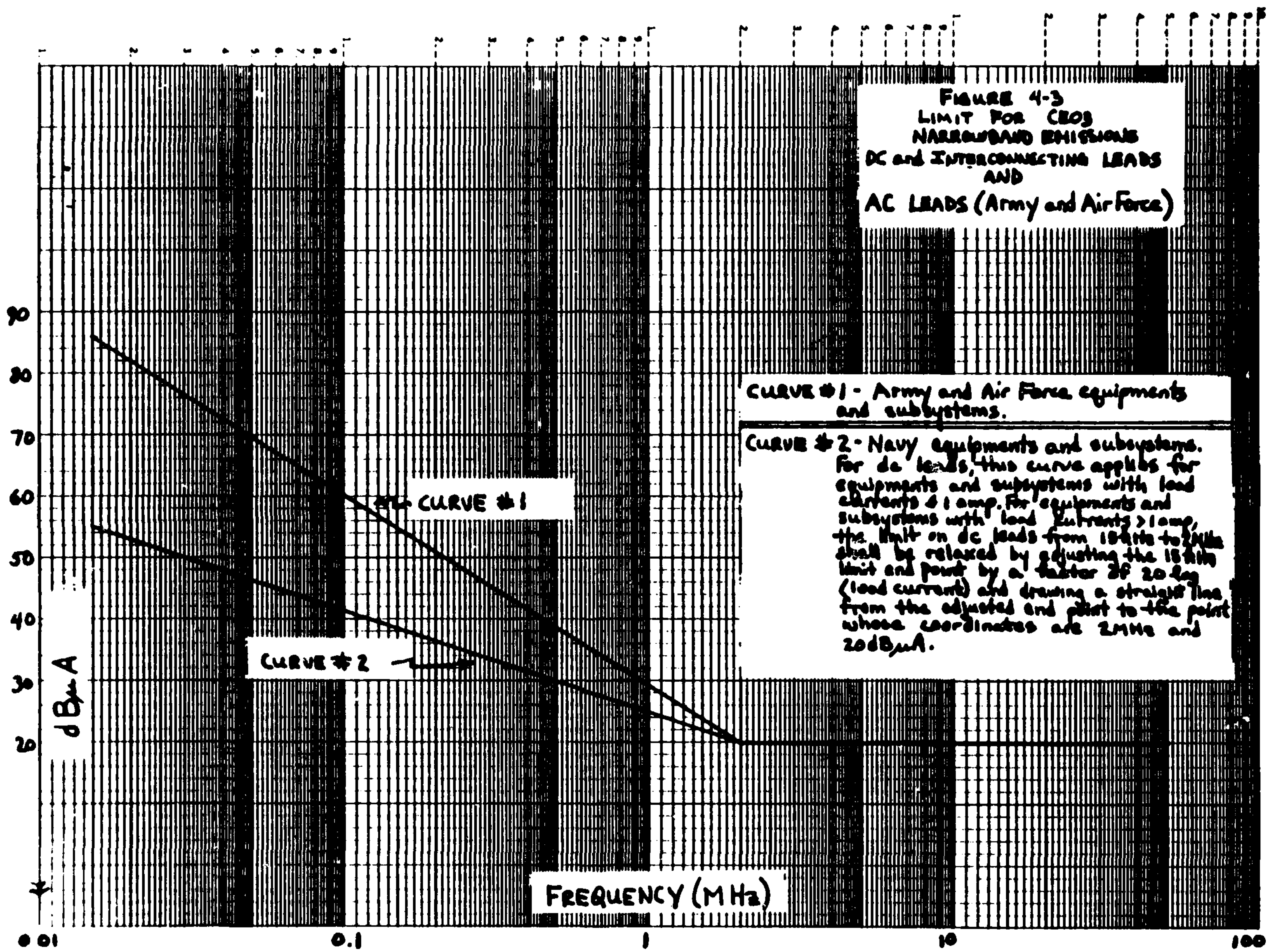
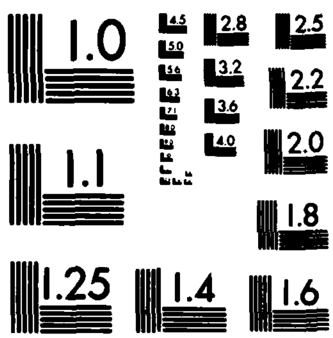


Figure A.2-2 LIMIT FOR CE03 NARROWBAND EMISSIONS - DC AND INTERCONNECTING LEADS

AD-A127 462 500-WATT SOLID-STATE RF POWER AMPLIFIER AM-7209( )/VRC 2/2
(U) E-SYSTEMS INC ST PETERSBURG FL ECI DIV M HARRIS
18 MAR 83 GO-61289 CECOM-82-C-J231 DAAB07-82-C-J231

UNCLASSIFIED F/G 17/2.1 NL



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

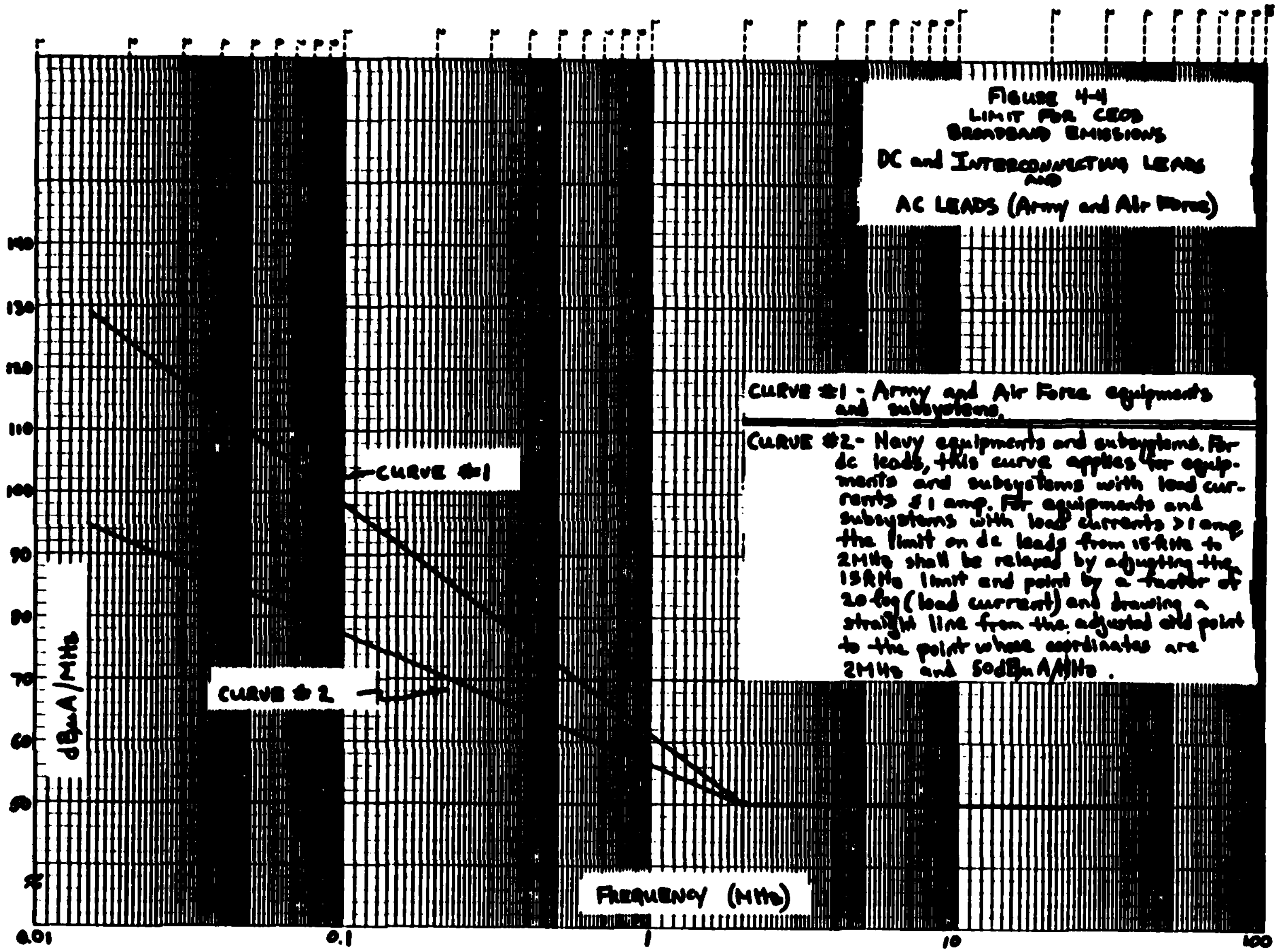


Figure A.2-3 LIMIT FOR CE03 BROADBAND EMISSIONS - DC AND INTERCONNECTING LEADS

A.2.5 CS01 - CONDUCTED SUSCEPTABILITY, POWER LEADS, 30 Hz TO 50 kHz

Amplifier response to externally-applied signals on the power lines is controlled by this requirement. The requirement states that the amplifier shall not malfunction or exhibit degraded performance or deviate beyond specified specified tolerances when energy is injected into the power leads at levels up to the limits of Figure A.2-4. An additional limit on the source energy is when the source, when set to dissipate 50 watts in 0.5 ohms cannot develop the required voltage at the input terminals, that level becomes the test limit.

A.2.6 CS02 - CONDUCTED SUSCEPTABILITY, POWER LEADS, 50 kHz TO 400 MHz

As with CS01, the equipment shall not malfunction, etc. when the amplifier power input terminals are subjected to a 1-volt signal from a 50-ohm source into a 50-ohm load with a 1-watt source limit into the 50-ohm load.

A.2.7 CS06 - CONDUCTED SUSCEPTABILITY, SPIKES, POWER LEADS

As with CS01, the DC power leads are subjected to an external spike and the equipment shall not malfunction, etc. The external signal for this requirement is a spike as defined in Figure A.2-5, with E1 equal to 100 volts and t1 less than or equal to 10 microseconds.

A.2.8 RE02 - RADIATED EMISSIONS, ELECTRIC FIELD, 14 kHz TO 10 GHz

This requirement relates to radiated narrowband and broadband electric field emissions from the amplifier case.

Narrowband requirements are shown in Figure A.2-6 and apply at the fundamental and all spurious and harmonic frequencies. Above 30 MHz, both horizontally and vertically polarized waves are limited.

Broadband requirements are shown in Figure A.2-7 and include radiated switching transients resulting from automatic cycling of electronic or electrical switching circuitry, keying of transmitters, or manual switching.

A.2.9 RS03 - RADIATED SUSCEPTABILITY, ELECTRIC FIELD, 14 kHz TO 10 GHz

The amplifier shall not malfunction, exhibit degraded performance, or deviate beyond specified tolerances when subjected to radiated electric fields (both vertical and horzontal polarization above 30 MHz) less than or equal to the following levels:

FREQUENCY RANGE (Hz)	"E" FIELD (V/M)	MODULATION CHARACTERISTICS
10 k - 2 M	1	AM, 50%, 1 kHz Tone
2 M - 30 M	5	AM, 50%, 1 kHz Tone
30 M - 76 M	10	FM, 8 kHz Dev., 1 kHz Tone
76 M - 400 M	10	AM, 50%, 1 kHz Tone
400 M - 2 G	10	Pulse, 0.1 microsecond, 400 PPS
2 G - 10 G	5	Pulse, 0.1 microsecond, 400 PPS

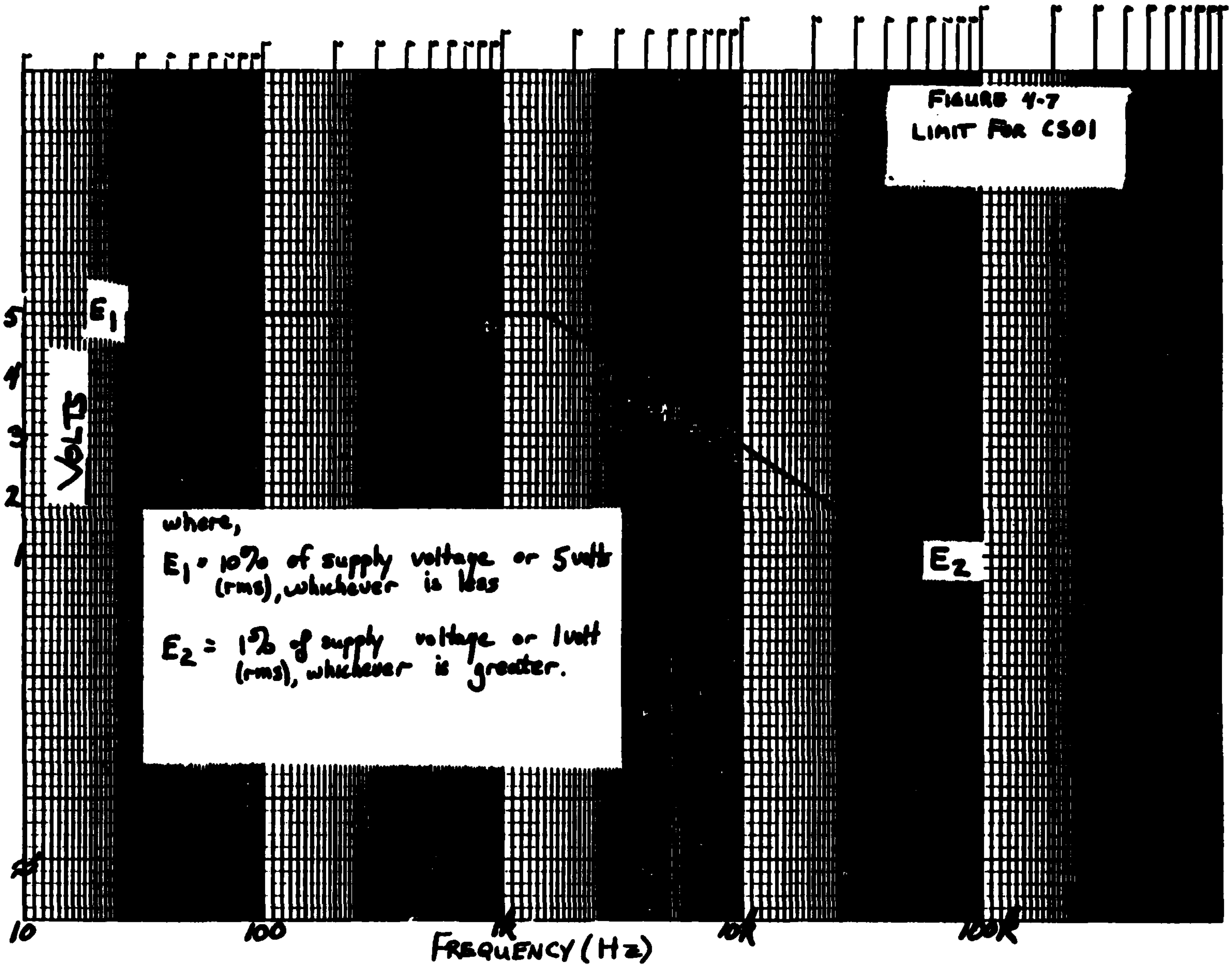


Figure A.2-4 LIMIT FOR CS01 CONDUCTED SUSCEPTABILITY ON POWER LEADS

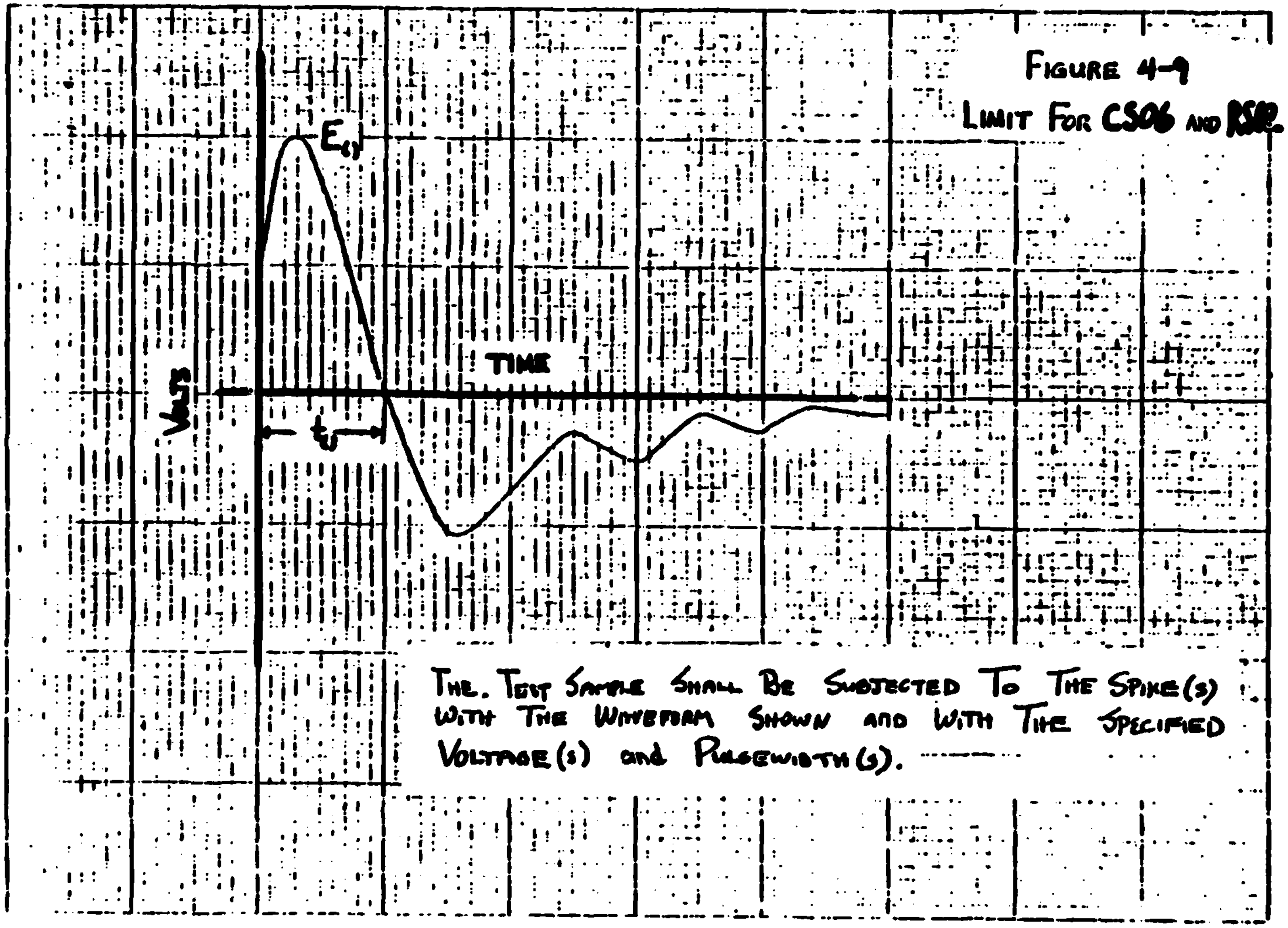


Figure A.2-5 LIMIT FOR CS06 CONDUCTED SUSCEPTABILITY TO SPIKES ON POWER LEADS

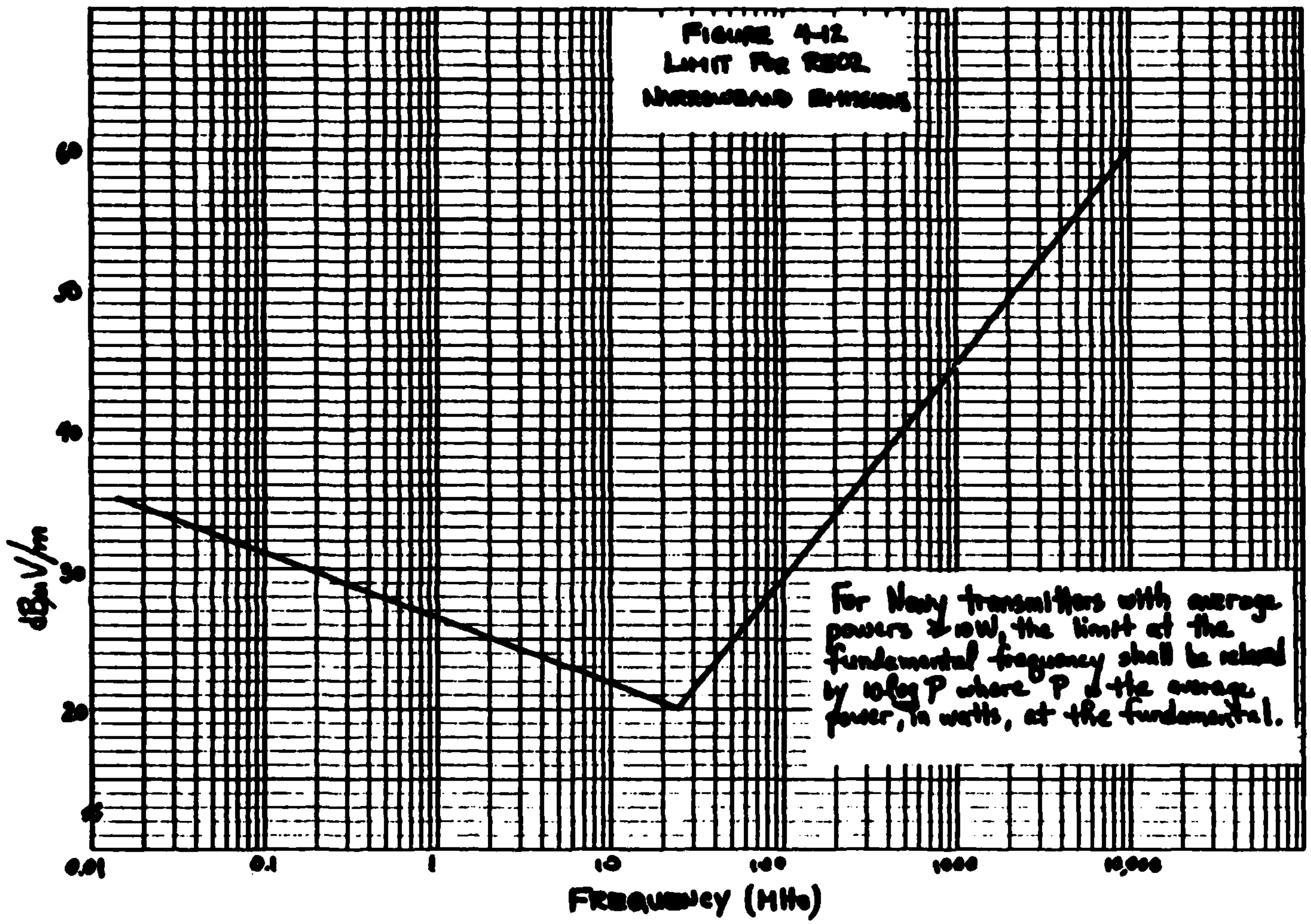


Figure A.2-6 LIMIT FOR RE02 NARROWBAND EMISSIONS

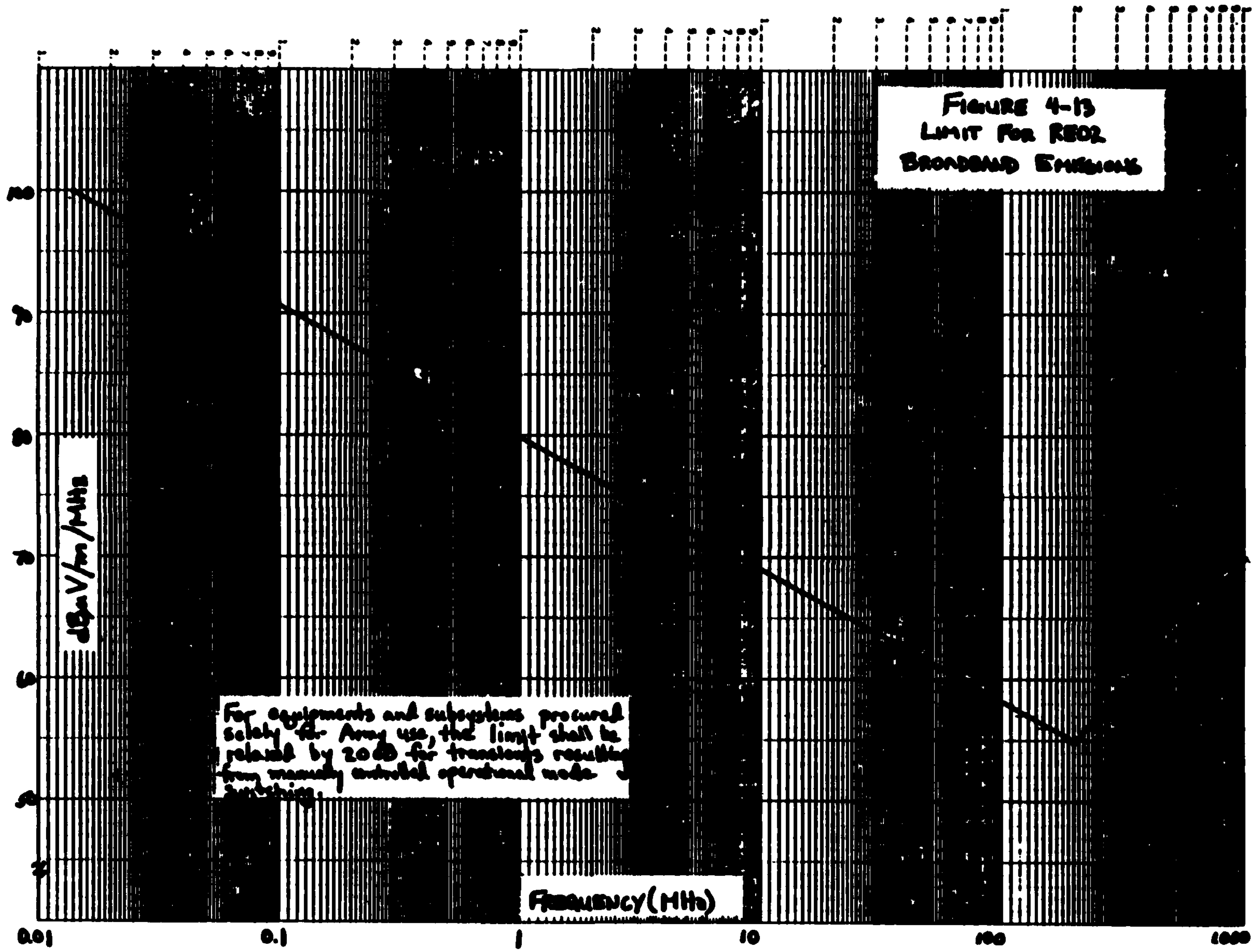


Figure A.2-7 LIMIT FOR RE02 BROADBAND EMISSIONS

APPENDIX A.3

MIL-STD-1275A SUMMARY

APPENDIX A.3

MIL-STD-1275A SUMMARY

A.3.1 INTRODUCTION

The characteristics of 28-volt military vehicle power supplies as described in MIL-STD-1275A (AT) and modified by the VHF amplifier specification are summarized below.

A.3.2 POWER SOURCE CHARACTERISTICS

Three "commonly-occurring" conditions exist: Fault-free including (1) Combined generator-battery supply or (2) Battery-only supply, and Single-fault including (3) Generator-only supply. An uncommon event is a multiple-fault condition where both the battery and generator regulator fail. Limits for the supply under these conditions are listed below.

	GENERATOR BATTERY	BATTERY ONLY	SINGLE FAULT	MULTIPLE FAULT
Steady-State Voltage[1] (V)				
Max	30	27	33	100
Min	25	20	0	0
Ripple (Figure A.3-1)				
Peak Voltage (+ and -) (V)	2	2	2	-
Frequency Range (Hz)	50-200 k	50-200 k	50-200 k	-
Surges				
Voltage (V)				
Max	40	100	100	-
Min	18	15	15	-
Impedance (mohms)	20	500	500	-
Figure No.	A.3-2	A.3-3	A.3-3	-
Spikes				
Peak Voltage (+ and -) (V)	250	250	250	-
Figure No.	A.3-4	A.3-4	A.3-5	-
Starting Disturbances				
Initial Engagement				
Min. Voltage (V)	6	6	-	-
Max. Time (Sec.)	1	1	-	-
Cranking Level				
Min. Voltage (V)	16	16	-	-
Max. Time (Sec.)	30	30	-	-

1. Equipment-specified operating voltage limits are 22-32 VDC, 27.5 VDC nominal.

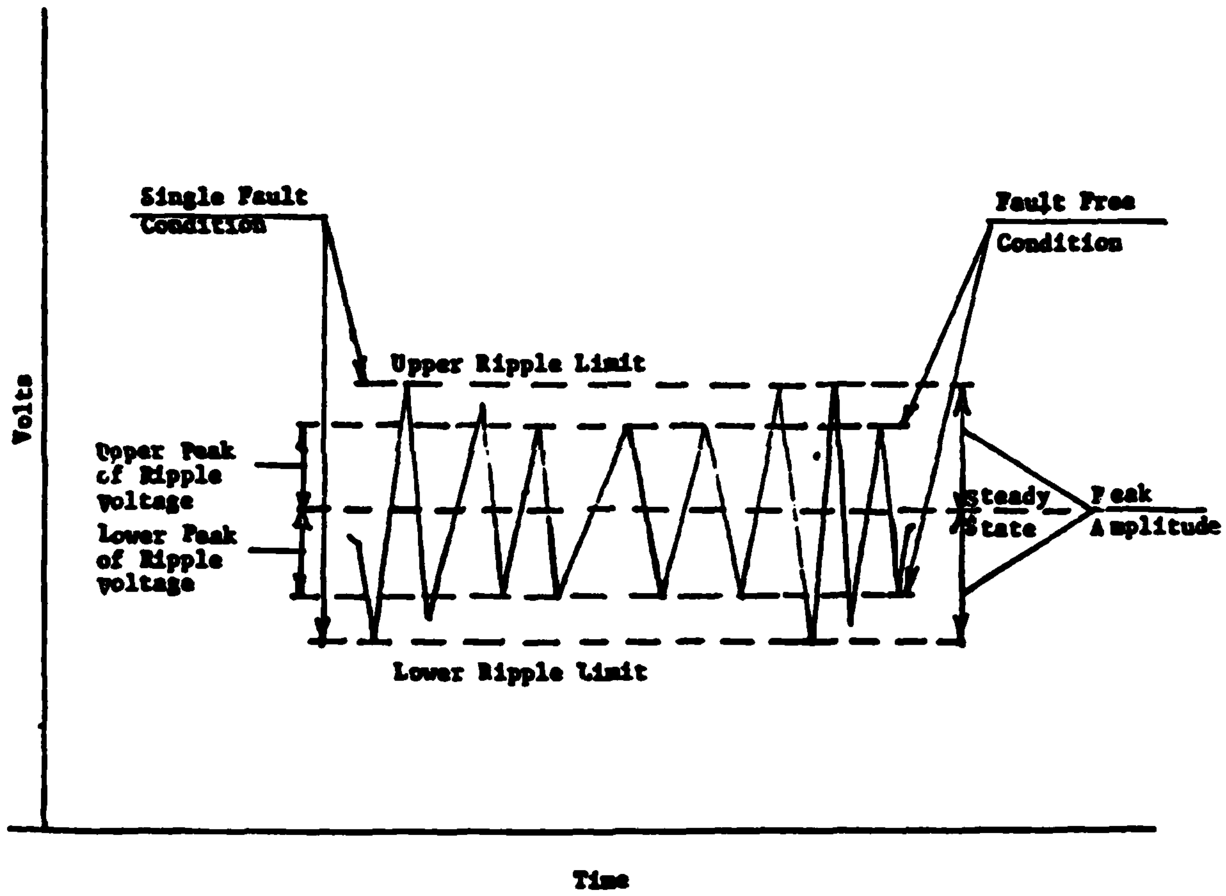


Figure A.3-1 RIPPLE VOLTAGE DEFINITIONS

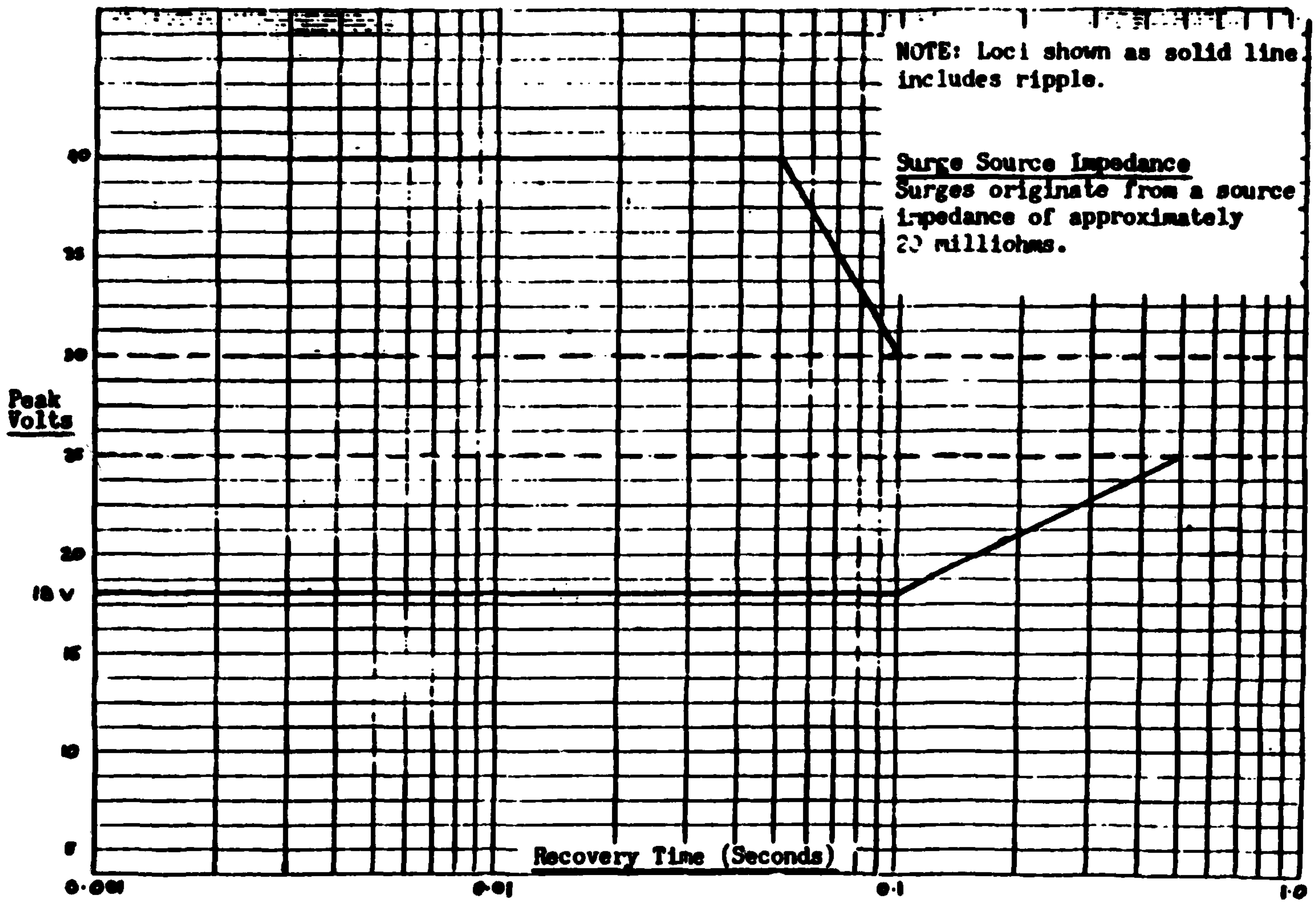


Figure A.3-2 SURGE VOLTAGE LIMITS - GENERATOR-BATTERY SOURCE

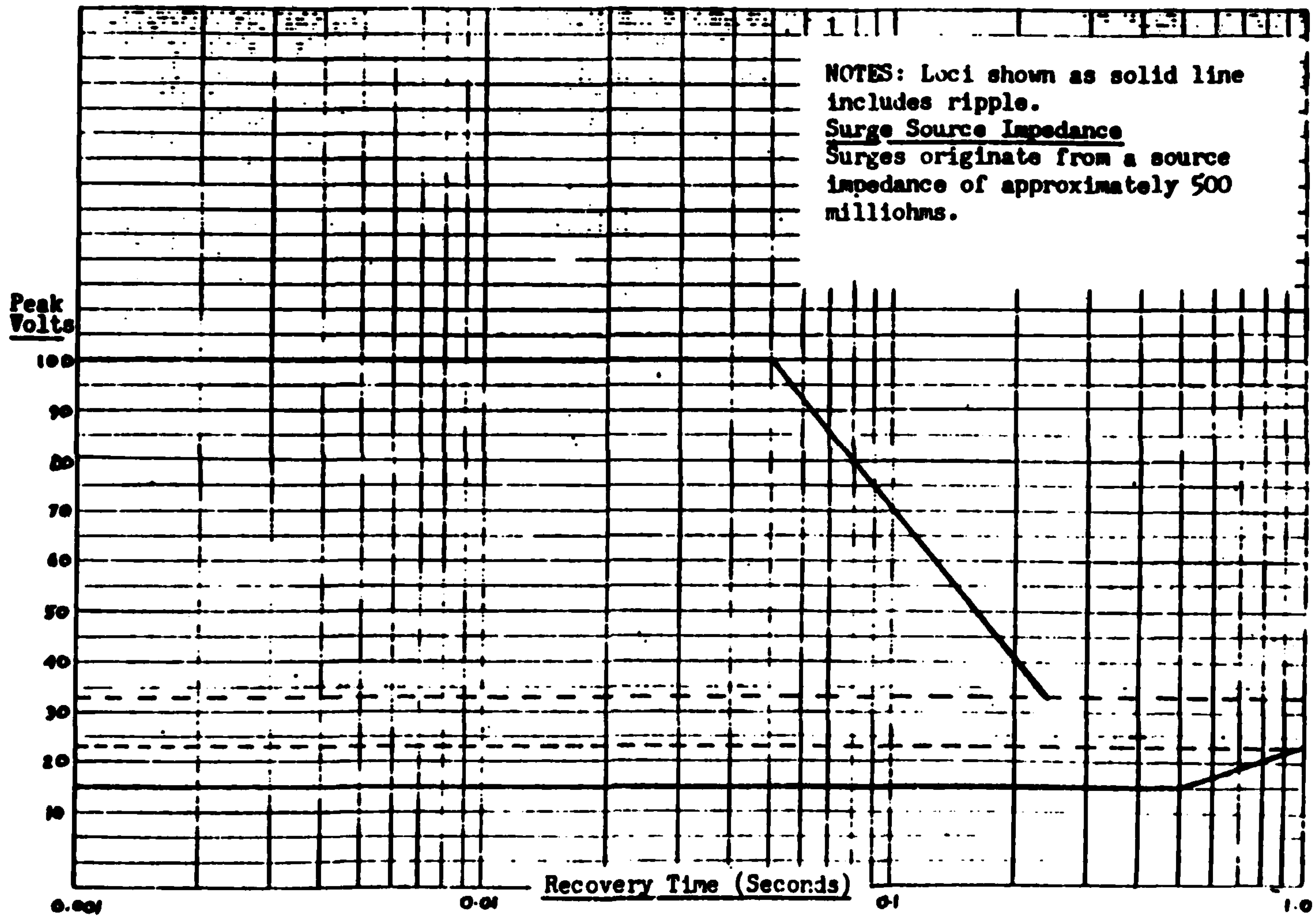


Figure A.3-3 SURGE VOLTAGE LIMITS - SINGLE-FAULT CONDITIONS

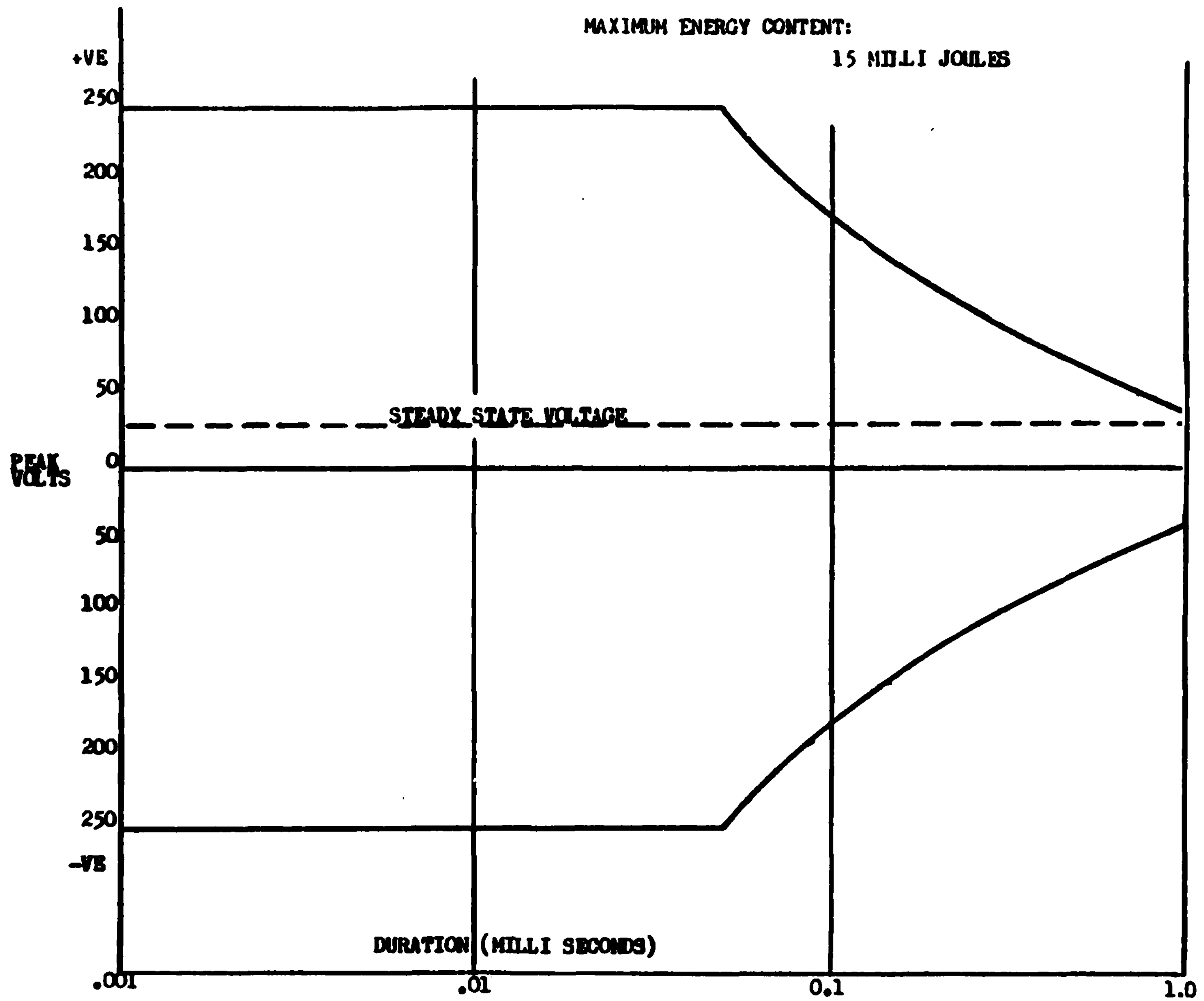


Figure A.3-4 SPIKE VOLTAGE LIMITS - BATTERY ON-LINE

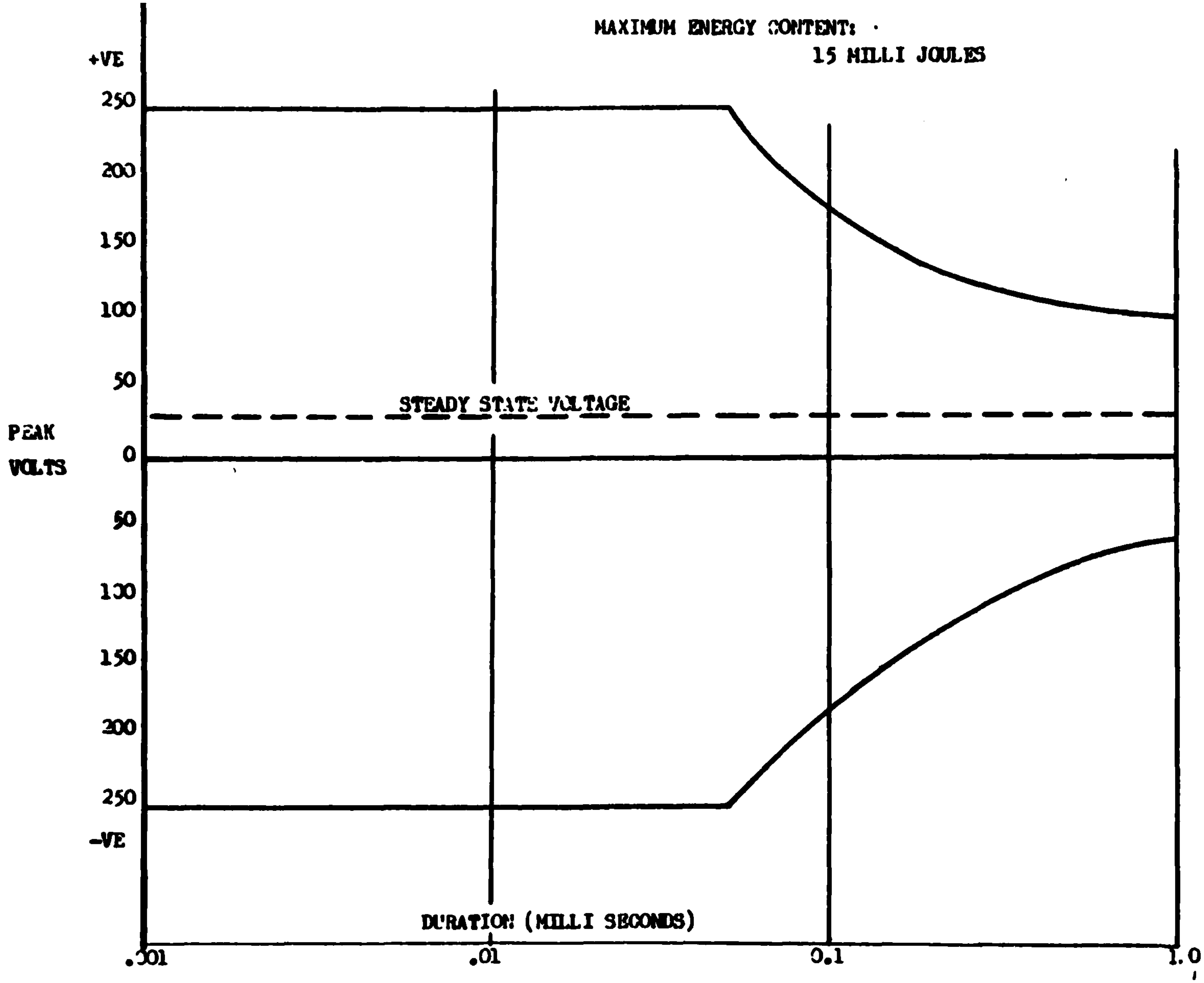


Figure A.3-5 SPIKE VOLTAGE LIMITS - SINGLE-FAULT CONDITION

APPENDIX A.4

RELIABILITY DERATING GUIDELINES

PARTS DERATING GUIDELINES & RELIABILITY LEVELS

PART TYPE	STRESS PARAMETER(s)	MINIMUM RELIABILITY LEVEL	DERATING REQUIREMENT MAX % OF RATED @ WORST CASE AMBIENT TEMP	REMARKS
Capacitors				
Ceramic (CKR)	Voltage	R	50 WVDC	1. Limit case temperature to 20°C below max. rated temp.
Mica (CMR)	Voltage	P	60 WVDC	2. DC plus peak AC shall not exceed derated WVDC (with ripple <75%).
Tantalum, Solid (CSR)	Voltage *	M	60 WVDC	3. Transients shall not exceed 80% of WVDC.
Tantalum, Non-Solid (CLR)	Voltage	M	70 WVDC	4. Current derated to 75% of rated.
Aluminum (CU)	Voltage	MIL-STD	70 WVDC	5. Peak AC voltage shall not exceed metallized plastic 20% of WVDC @ 60 Hz, 15% of WVDC @ 120 Hz, 1% of WVDC @ 10 kHz. For all other dielectrics 60% of WVDC.
Ceramic, Glass(PC) Variable (CV)	Voltage	MIL-STD	90 WVDC	* Maintain 3 Ω/volt series resistance between power source and capacitor
Fixed (CTR)	Voltage	P	50 WVDC	

PARTS DERATING GUIDELINES & RELIABILITY LEVELS

PART TYPE	STRESS PARAMETER(s)	MINIMUM RELIABILITY LEVEL	DERATING REQUIREMENT MAX % OF RATED @ WORST CASE AMBIENT TEMP	REMARKS
Diodes				
Rectifier and Switching	Forward Current Reverse Current Peak Surge Current	JAN	70 70 (85 with transients) 75	Junction temp. shall not exceed 70% of T_j max. under worst case electrical and thermal conditions.
Regulator, Zener and Voltage Reference	Forward Current Peak Surge Current	JAN	70 75	
Relays				
All Types	Current Under Make, Break and Carry Conditions	MIL-STD	75 with resistive load 50 with inductive load	1. Peak in-rush shall not exceed rated value. 2. Minimum coil current must be maintained. 3. Suppress arching by paralleling load with absorbing ckts. 4. Derate to 80% of maximum temperature.

PARTS DERATING GUIDELINES & RELIABILITY LEVELS

PART TYPE	STRESS PARAMETER(s)	MINIMUM RELIABILITY LEVEL	DERATING REQUIREMENT MAX % OF RATED @ WORST CASE AMBIENT TEMP	REMARKS
Integrated Circuits				
Digital	Fanout Current	Class B **	80 of max. rated. For devices interfacing with different families or discrete devices, derate output sink current to 80% of max. rating.	Unused pins specified as "non-connection" (NC) should be connected to ground, as applicable. Under certain conditions, unused input pins may be clipped to improve noise immunity.
Linear	Turn-on, Turn-off Voltage Transients	Class B **	90	** When a 38510 Class "B" IC is not available, the alternate IC will be screened to MIL-STD-883 Class "B".
	Differential Input Voltage		90	Devices shall be operated at Vcc vendor recommended value.
	Output Current		80	
	Junction Temp. (T_J) Max.		70	
	Operating Frequency		60	
RFI Filters				
All Types	Current Voltage	JAN	75 75	

PA ATING GUIDELINES & RELIABILITY LEVELS

PART TYPE	STRESS PARAMETER(s)	MINIMUM RELIABILITY LEVEL	DERATING REQUIREMENT MAX % OF RATED @ WORST CASE AMBIENT TEMP	REMARKS
Switches				
All Types	Current	MIL-STD	50	Derate to 80% of max. temperature.
Transistors				
Power	Junction Temperature (T_j)	JAN	70 of the junction temp. (T_j) max. under worst case electrical & thermal conditions	Stress shall be within the supplier safe operating limits considering all transients.
RF Power	Junction Temperature (T_j)	JAN	70 of the junction temp. (T_j) max. under worst case electrical & thermal conditions	
All Other	Voltage Current Junction Temp. (T_j)	JAN	70 (90 with transient) 75 70 of T_j max. under worst case electrical and thermal conditions	

PARTS DERATING GUIDELINES & RELIABILITY LEVELS

PART TYPE	STRESS PARAMETER(s)	MINIMUM RELIABILITY LEVEL	DERATING REQUIREMENT MAX % OF RATED @ WORST CASE AMBIENT TEMP	REMARKS
Wire & Cable				
Insulated Electrical Wire	Current DWV	MIL-STD	75 75	Derate to 40% for wire bundles of 15 or more.
Connectors				
Electrical Circular and Rectangular	Contact Current Working Voltage	MIL-STD	60 25	Mounting surface temp. limited to 80% of maximum.
Magnetics				
Inductors	Voltage Between Windings or Windings to Case	MIL-STD	80 (90 with transient)	Ambient plus hot spot temp. rise $\leq$ 15°C below maximum insulation temp. rating.
	Current		70	
Transformer				
Audio & Power	Voltage Between Windings or Windings to Case	MIL-STD	80 (90 with transient)	
	Current		70	
Pulse, Low Power, RF	Voltage Between Windings or Windings to Case	MIL-STD	70 (90 with transient)	
	Current		60	

PARTS DERATING [illegible]NES & RELIABILITY LEVELS

PART TYPE		STRESS PARAMETER(s)	MINIMUM RELIABILITY LEVEL	DERATING REQUIREMENT MAX % OF RATED @ WORST CASE AMBIENT TEMP	REMARKS
<u>Resistors</u>					
Carbon Comp.	(RCR)	Power Voltage	S	80 80	Limit temp. to 80% of max.
Film, General Purpose	(RLR)	Power Voltage	S	80 80	
Film, High Stability	(RNC) (RNR)	Power Voltage	R	80 80	
Wirewound Power	(RWR)	Power Voltage	R	70 80	
Wirewound	(RER)	Power Voltage	P	70 80	
Variable, Composition	(RV)	Power Voltage	MIL-STD	60 80	
Variable, Non-Wirewound	(RVC)	Power Voltage	MIL-STD	60 80	
Variable, Wirewound	(RTR)	Power Voltage	P	60 80	
Variable, Non-Wirewound	(RJR)	Power Voltage	P	60 80	
Networks, Fixed Film	(RZ)	Power Voltage	MIL-STD	60 80	
Accurate, Fixed Wirewound	(RBR)	Power Voltage	R	70 80	

FILM